JADARD

JD9613

Data Sheet

240RGB x 360 dot, Full color,
with internal GRAM, LTPS AMOLED Single Chip Driver

Preliminary Version 0.02
2021/3/25

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1. Revision History

Version	Date	Description of modification
0.00	2020/11/20	New setup
0.01	2021/01/21	1. Modify the logo 2. Add Swire , OLED_EN pin 3. Modify the layout resistance 4. Modify the Absolute maximum rating

2. General Description

The JD9613 is a 262,144-color single-chip SOC driver for LTPS AMOLED display with flexible resolution of 2x(Horizontal) , 2x(Vertical), comprising a 120-channel source driver, GRAM for graphic display data, and power supply circuit.

The JD9613 supports MIPI-DSI interface, Quad SPI interface , parallel 8bit data bus MCU interface, 3-/4-line serial peripheral interface (SPI) and 2 lane SPI data transmission. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The JD9613 can operate with 1.65V ~ 3.6V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an AMOLED. The JD9613 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities.JD9613 supports full color, 262k color , 65k color , 256 color ,8-color display mode and sleep mode for precise power control by software and these features make the JD9613 an ideal AMOLED driver for wearable device application , including I-watch and smart band.

3. Features

3.1. Display

- Single chip solution for a AMOLED display
  - Resolution:
    - 240RGBx240
    - 180RGBx300
    - 128RGBx360
    - 240RGBx360
    - 216RGBx400
    - Above range: 2*N*RGBx2M
- Display color modes
  - Full color mode:
    - 16.7M colours (24-bit 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colours (18-bit 6(R):6(G):6(B))
    - 65k colours (16-bit 5(R):6(G):5(B))
    - 256 colours (8-bit 3(R):3(G):2(B))
    - 8 colours (3-bit 1(R):1(G):1(B))

3.2. Display interface

- Display interface types supported
  - 8bits 80-series MCU interface
  - Serial peripheral interface(SPI)
  - Dual serial peripheral interface(Dual SPI)
  - Quad serial peripheral interface(Quad SPI)
  - MIPI Display Serial Interface (1 lane only, Maximum bit rate is 250Mbps)
    - Support DSI Version 1.1
    - Support D-PHY version 1.00

3.3. Input voltage ranges

- I/O and interface power supply (IOVCC): 1.65V to 3.3V
- High speed interface power supply (VCC): 1.65V to 3.3V
- DC/DC set-up supply (VCIB): 2.7V to 3.3V
- Analog power supply (VCIR): 2.7V to 3.3V
- OTP programming voltage (VOTP pin): Feed 8.3V ± 0.1V

3.4. Output voltage ranges

- On module DC/DC converter
  - Source output voltage level: VGMP= +2.0V to 6.3V (Max. VGMP <= AVDD - 0.5V)
    VGSP= +0.2V to 4.5V
  - Positive gate driver output voltage level: VGHR= +3.0V to 10.5V
  - Negative gate driver output voltage level: VGLR= -2.0 to -9.0V

3.5. Miscellaneous of chip

- Internal level shifter for Gate Driver control
- Support R/G/B separate Digital Gamma Correction function
- Internal Oscillator generation
- Source output MUX 1-6 /1-12 with 120ch source output pins
- Control external power IC by one-wire interface
- Temperature range: -20 to +85 °C
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 2 times OTP for Digital Gamma Correction setting
- 2 times OTP for VGMP/VGSP setting
- 5 times OTP for ID setting
- Support ACL/BC function
- Support over voltage/current protection function
- Support detect panel break function
-

4. Device Overview

4.1. Block Diagram

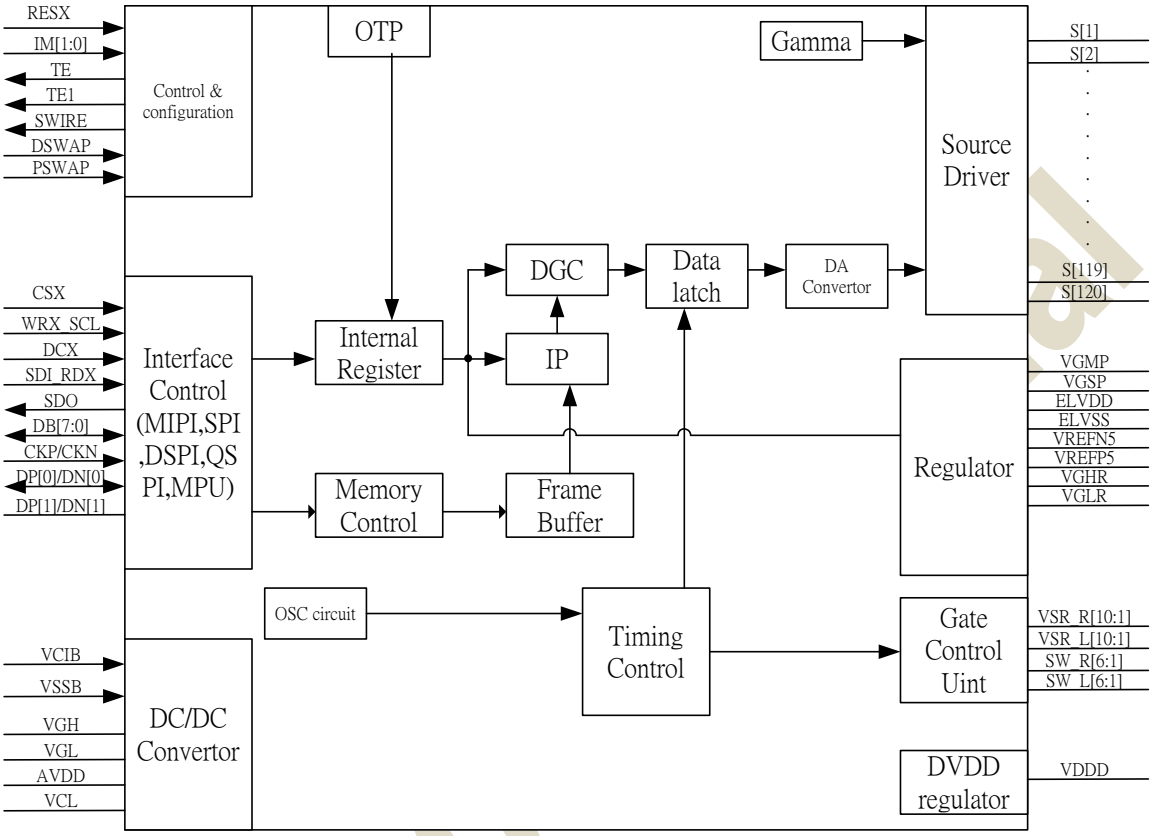


Figure 4.1 Block diagram

4.2. AMOLED power generation scheme

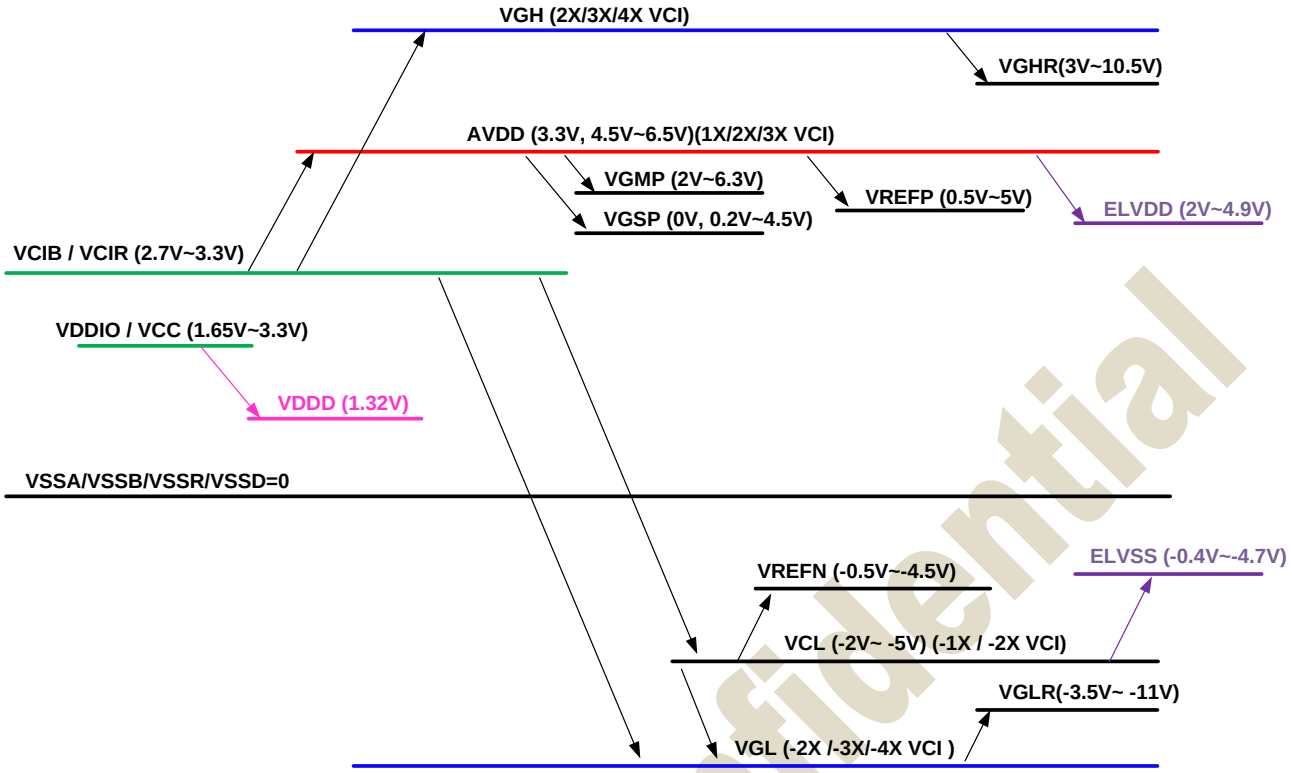


Figure 4.2 AMOLED power generation scheme

4.3. Output voltage range

JD9613 generates corresponding voltage with LTPS AMOLED panel by internal power supply circuit. Please set up each voltage output according to the AMOLED panel.

Name	Function	Set up value	Note
AVDD	DC/DC converter circuit output		Reference register
VGH	DC/DC converter circuit output		Reference register
VGL	DC/DC converter circuit output		Reference register
VCL	DC/DC converter circuit output		Reference register
VGHR	Positive gate driver output voltage level		Reference register
VGLR	Negative gate driver output voltage level		Reference register
VREFP5	OLED pixel reference voltage		Reference register
VREFN5	OLED pixel reference voltage		Reference register
ELVDD	Positive OLED power		Reference register
ELVSS	Negative OLED power		Reference register
VGMP	Reference voltage for gamma circuit		Reference register
VGSP	Reference voltage for gamma circuit		Reference register
VDDD	Digital power for internal digital circuit.	+1.32V	

Table 4.1 Voltage configuration

4.4. DC/DC Converter Circuit

4.4.1. Power Mode 1 (ELVDD/ELVSS supply by internal power circuit)

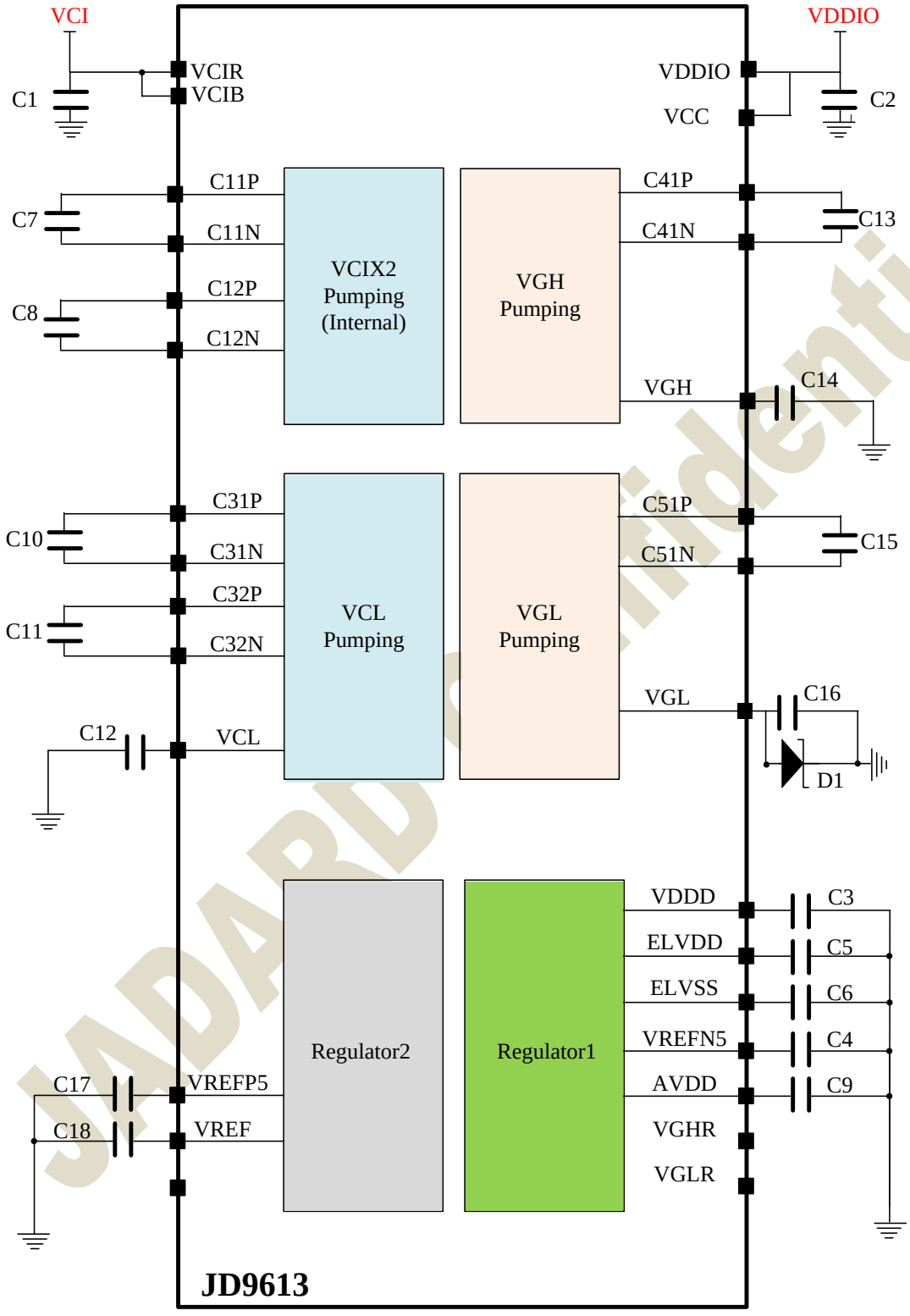


Figure 4.3 3 ELVDD/ELVSS supply by internal power circuit

4.4.2. External component table for Power Mode 1 (ELVDD/ELVSS supply by internal power circuit)

Pad Name	Symbol	Connection	Typical Value
VCIR / VCIB	C1	Connect to Capacitor : VCIR/VCIB ---(+)----| |--- (-)-----VSSR	6.3v/ 2.2 μF
C11P – C11N	C7	Connect to Capacitor : C11P ---(+)----| |--- (-)-----C11N	10v/1.0 μF
C12P – C12N	C8	Connect to Capacitor : C12P ---(+)----| |--- (-)-----C12N	10v/1.0 μF
C31P – C31N	C10	Connect to Capacitor : C31P ---(+)----| |--- (-)-----C31N	6.3v/1.0 μF
C32P – C32N	C11	Connect to Capacitor : C32P ---(+)----| |--- (-)-----C32N	6.3v/1.0 μF
AVDD	C9	Connect to Capacitor : AVDD ---(+)----| |--- (-)-----VSSR	10v/2.2 μF
C41P – C41N	C13	Connect to Capacitor : C41P ---(+)----| |--- (-)-----C41N	16v/1.0 μF
C51P – C51N	C15	Connect to Capacitor : C51P ---(+)----| |--- (-)-----C51N	16v/1.0 μF
VDDIO/VCC	C2	Connect to Capacitor: IOVCC/VCC ---(+)----| |--- (-)----- VSSD	6.3v/1.0 μF
VCL	C12	Connect to Capacitor: VCL ---(-)----| |--- (+)----- VSSB	10v/2.2 μF
VREF	C18	Connect to Capacitor: VREF ---(-)----| |--- (+)----- VSSR	6.3v/22nF
VREFP5	C17	Connect to Capacitor: VREFP5 ---(-)----| |--- (+)----- VSSR	10v/1.0 μF
VREFN5	C4	Connect to Capacitor: VREFN5 ---(-)----| |--- (+)----- VSSR	10v/1.0 μF
VGH	C14	Connect to Capacitor: VGH ---(+)----| |--- (-)-----VSSB	25V/2.2 μF
VGL	C16	Connect to Capacitor: VGL ---(-)----| |--- (+)----- VSSB	25V/2.2 μF
	D1	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►∫--- (+)---- VSSB	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
ELVDD	C5	Connect to Capacitor: ELVDD---(-)----| |--- (+)-----VSSA	10v/2.2 μF
ELVSS	C6	Connect to Capacitor: E:VSS ---(+)----| |--- (-)-----VSSA	10v/2.2 μF
VDDD	C3	Connect to Capacitor: VDDD ---(+)----| |--- (-)-----VSSD	6.3v/2.2 μF

4.4.3. Power Mode 2 (ELVDD/ELVSS supply by external power circuit)

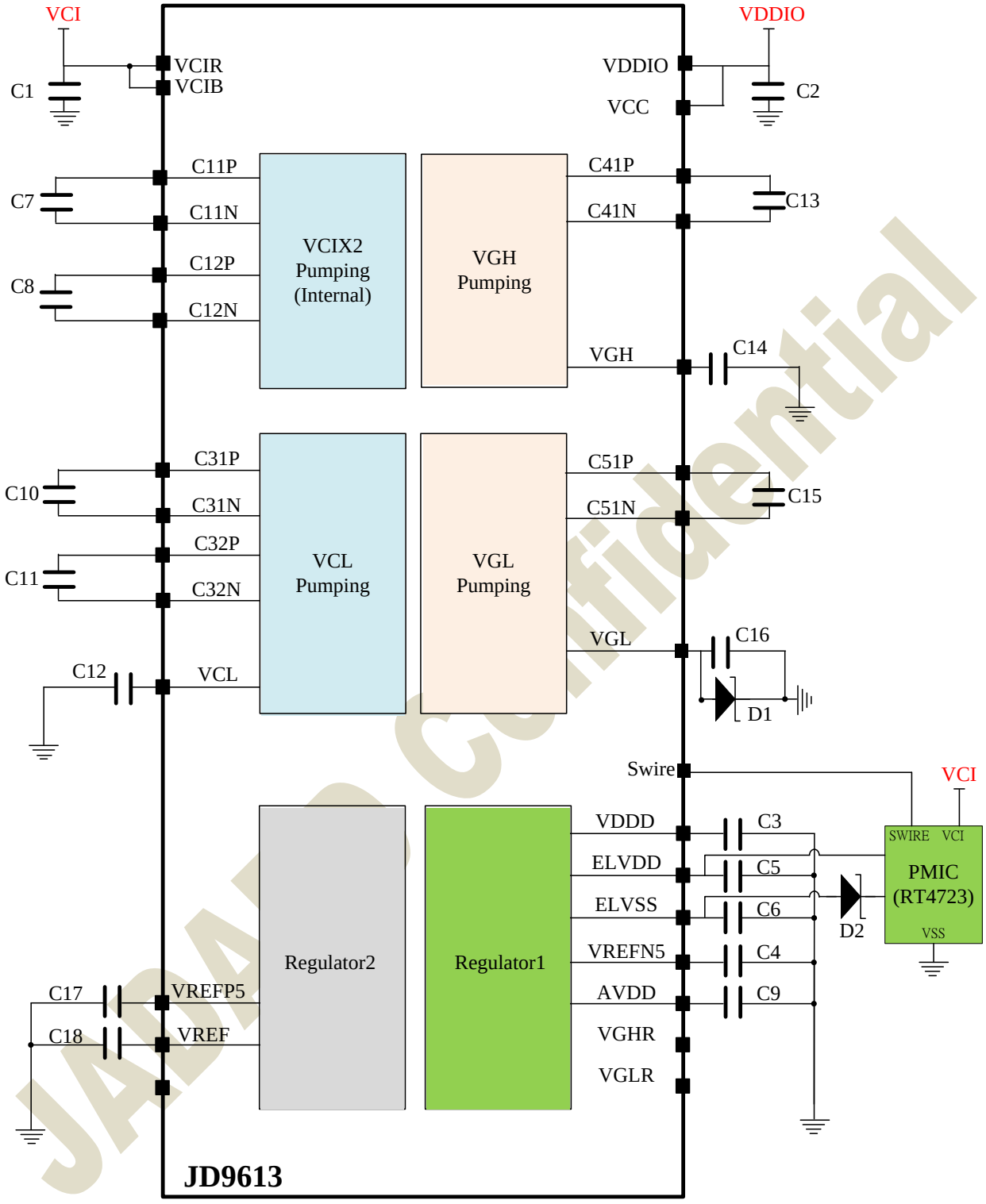


Figure 4.4 ELVDD/ELVSS supply by RT4723

4.4.4. External component table for Power mode 2 (ELVDD/ELVSS supply by external power circuit)

Pad Name	Symbol	Connection	Typical Value
VCIR / VCIB	C1	Connect to Capacitor : VCIR/VCIB ---(+)----| |--- (-)-----VSSR	6.3v/ 2.2 μF
C11P – C11N	C7	Connect to Capacitor : C11P ---(+)----| |--- (-)-----C11N	10v/1.0 μF
C12P – C12N	C8	Connect to Capacitor : C12P ---(+)----| |--- (-)-----C12N	10v/1.0 μF
C31P – C31N	C10	Connect to Capacitor : C31P ---(+)----| |--- (-)-----C31N	6.3v/1.0 μF
C32P – C32N	C11	Connect to Capacitor : C32P ---(+)----| |--- (-)-----C32N	6.3v/1.0 μF
AVDD	C9	Connect to Capacitor : AVDD ---(+)----| |--- (-)-----VSSR	10v/2.2 μF
C41P – C41N	C13	Connect to Capacitor : C41P ---(+)----| |--- (-)-----C41N	16v/1.0 μF
C51P – C51N	C15	Connect to Capacitor : C51P ---(+)----| |--- (-)-----C51N	16v/1.0 μF
VDDIO/VCC	C2	Connect to Capacitor: IOVCC/VCC ---(+)----| |--- (-)----- VSSD	6.3v/1.0 μF
VCL	C12	Connect to Capacitor: VCL ---(-)----| |--- (+)----- VSSB	10v/2.2 μF
VREF	C18	Connect to Capacitor: VREF ---(-)----| |--- (+)----- VSSR	6.3v/22nF
VREFP5	C17	Connect to Capacitor: VREFP5 ---(-)----| |--- (+)----- VSSR	10v/1.0 μF
VREFN5	C4	Connect to Capacitor: VREFN5 ---(-)----| |--- (+)----- VSSR	10v/1.0 μF
VGH	C14	Connect to Capacitor: VGH ---(+)----| |--- (-)-----VSSB	25V/2.2 μF
VGL	C16	Connect to Capacitor: VGL ---(-)----| |--- (+)----- VSSB	25V/2.2 μF
	D1	Connect to Schottky Diode(VR≥30V): VGL ---(-)----►∫--- (+)---- VSSB	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
ELVDD	C5	Connect to Capacitor: ELVDD---(-)----| |--- (+)-----VSSA	10v/2.2 μF
ELVSS	C6	Connect to Capacitor: E:VSS ---(+)----| |--- (-)-----VSSA	10v/2.2 μF
	D2	Connect to Schottky Diode(VR≥30V): ELVSS ---(-)----►∫--- (+)---- ext PMIC	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
VDDD	C3	Connect to Capacitor: VDDD ---(+)----| |--- (-)-----VSSD	6.3v/2.2 μF

Maximum layout resistance

Name	Pin Definition	Maximum series resistance	Unit
IOVCC, VCC	Power supply	3	Ω
VCIR, VCIB	Power supply	3	Ω
VSSD, VSSA,VSSR,VSSB	Power supply	3	Ω
VOTP	OTP Power supply	20	Ω
TEST_OSC, RDX, TESTP, TESTN	Input	100	Ω
D[7:0]	Input	100	Ω
CSX,WRX_SCL, SDI_RDX, DCX,RESX	Input	100	Ω
DSWAP, PSWAP, IM[1:0]	Input	100	Ω
SDO, TE, TE1, SWIRE,OLED_EN	Output	100	Ω
DP[0],DN[0]	Input + Output	6	Ω
DP[1],DN[1]	Input	6	Ω
CKP,CKN	Input	6	Ω
VGSP, VGMP,VREFN5,VREFP5	Output, Capacitor Connection	10	Ω
VDDD	Output, Capacitor Connection	5	Ω
AVDD, VCL	Output, Capacitor Connection	10	Ω
VREF	Output, Capacitor Connection	20	Ω
VGH, VGL, VGL, VGHR, VGLR,	Output, Capacitor Connection	10	Ω
C11P, C11N, C12P, C12N C31P, C31N, C32P, C32N, C41P, C41N, C51P, C51N	Capacitor Connection	4	Ω

Table 0.1 Maximum Layout Resistance

5. Pin description

<table>
<tr><th colspan="4">Host interface pins</th></tr>
<tr><th>Pin name</th><th>I/O type</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM1 ~ IM0</td><td>I</td><td>VSSD / IOVCC</td><td>Select the Interface mode as listed below:
<table>
<tr><th>IM1</th><th>IM0</th><th>Command / Display Data</th><th>Data Pin</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">0</td><td>MIPI</td><td>CKP/N, DP[0]/DN[0], DP[1]/DN[1]</td></tr>
<tr><td>3-wire SPI</td><td>SDI_RDX, SDO</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td>MIPI</td><td>CKP/N, DP[0]/DN[0], DP[1]/DN[1]</td></tr>
<tr><td>4-wire SPI</td><td>SDI_RDX, SDO</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">0</td><td>MIPI</td><td>CKP/N, DP[0]/DN[0], DP[1]/DN[1]</td></tr>
<tr><td>Quad SPI</td><td>SDI_RDX, SDO, DCX, DB[1:0]</td></tr>
<tr><td>1</td><td>1</td><td>MCU 8bits</td><td>DB[7:0]</td></tr>
</table>
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>DSWAP, PSWAP</td><td>I</td><td>VSSD / IOVCC</td><td>Select for DSI data lane sequence and polarity.
<table>
<tr><th>Pad Name</th><th>DP[0]</th><th>DN[0]</th><th>CKP</th><th>CKN</th><th>DP[1]</th><th>DN[1]</th></tr>
<tr><td>DSWAP=0
PSWAP=0</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>NA</td><td>NA</td></tr>
<tr><td>DSWAP=0
PSWAP=1</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>NA</td><td>NA</td></tr>
<tr><td>DSWAP=1
PSWAP=0</td><td>NA</td><td>NA</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>DSWAP=1
PSWAP=1</td><td>NA</td><td>NA</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td></tr>
</table>
Note: 1 lane only.</td></tr>
<tr><td>DP[0],
DN[0]</td><td>I/O</td><td>DSI Host</td><td>MIPI-DSI Data differential signal input pins. (Data lane 0)
if not used , Please connected to VSSD or .open</td></tr>
<tr><td>CKP,
CKN</td><td>I</td><td>DSI Host</td><td>MIPI-DSI CLOCK differential signal input pins.
if not used , Please connected to VSSD or open.</td></tr>
<tr><td>DP[1],
DN[1]</td><td>I/O</td><td>DSI Host</td><td>MIPI-DSI Data differential signal input pins. (Data lane01)
If not used , Please connected to VSSD or open.</td></tr>
<tr><td>TE, TE1</td><td>O</td><td>Host</td><td>Tearing effect output pin to synchronize host to frame writing, activated by S/W command.
-If not used, open this pin.</td></tr>
<tr><td>Swire</td><td>O</td><td>DC/DC PMIC</td><td>Swire protocol setting pin for PMIC ,
-If not used, open this pin.</td></tr>
<tr><td>OLED_EN</td><td>O</td><td>DC/DC PMIC</td><td>Power IC enable control pin</td></tr>
</table>

			-If not used, open this pin.
RESX	**I**	**Host**	Reset pin. Must be reset after power is supplied (**Signal is active low.**).
CSX	**I**	**Host**	Chip select pin. 0(GND): chip can be accessed; 1(IOVCC): chip cannot be accessed. If this pin is not used, please connect it to IOVCC.
DCX	**I**	**Host**	Data/command selection pin in parallel interface. When DCX='1', data is selected. When DCX='0', command is selected. Data/command selection pin in 4-line serial interface. Second Data lane in 2 data lane serial interface. **If not used, this pin should be connected to IOVCC.**
WRX_SCL	**I**	**Host**	Write enable in MCU parallel interface. This pin is used to be serial interface clock. **If not used, this pin should be connected to IOVCC.**
SDI_RDX	**I**	**Host**	Read enable in 8080 MCU parallel interface or Data input in SPI interface. The data is latched on the rising edge of the WRX_SCL signal in SPI interface. **If not used, this pin should be connected to IOVCC or GND..**
SDO	**O**	**Host**	Serial data output. Let it to open in DSI interface mode.
DB[7:0]	I/O	**Host**	DB[7:0] are used as MCU parallel interface data bus. DB[1:0] are used as Quad SPI interface data bus If not used, this pin should be connected to IOVCC or GND.
Panel driver output			
S[1] ~ S[120]	**O**	**OLED**	Output voltages applied to the OLED.
SDMY1~ SDMY16	**O**	**OLED**	Dummy pad, Let it open.
VSR_L[10:1] VSR_R[10:1]	**O**	**OLED**	These pins are used for GIP control signal. If not use, let it open.
SW_L[6:1] SW_R[6:1]	**O**	**OLED**	These pins are used for switch control signal. If not use, let it open.
SD_PASS1 SD_PASS2	**O**	**OLED**	Dummy pad, Let it open.

Power supply pins			
VCIB	**I**	**Power IC**	Power supply for DC/DC converter
VCIR	**I**	**Power IC**	Power supply for regulator/analog system VDDB,VDDA and VDDR should be the same input voltage level.
IOVCC	**I**	**Power IC**	Power supply for interface system except MIPI interface
VCC	**I**	**Power IC**	Power supply for DVDD regulator
VSSB	**I**	**Power IC**	System ground for DC/DC convertor
VSSA	**I**	**System ground**	System ground for Source OP system
VSSR	**I**	**System ground**	System ground for regulator system
VSSD	**I**	**System ground**	System ground for interface, digital system and internal MIPI analog system
VOTP	**I**	**Power IC or Open**	External high voltage pin used in OTP mode and operates at 8.3V. If not used, let this pin open.
AVDD	**O**	**Capacitor**	DC/DC converter circuit output .Connect a capacitor for stabilization.
VCL	**O**	**Capacitor**	DC/DC converter circuit output. Connect a capacitor for stabilization.
VGH	**O**	**Capacitor**	DC/DC converter circuit output .Connect a capacitor for stabilization.
VGL	**O**	**Capacitor**	DC/DC converter circuit output .Connect a capacitor for stabilization.
VGHR	**O**	**Capacitor**	Regulator output voltage generated from VGH. Connect to a stabilizing capacitor between AVSS and VGHR. If not used, please open.
VGLR	**O**	**Capacitor**	Regulator output voltage generated from VGL. Connect to a stabilizing capacitor between AVSS and VGLR. If not used, please open.
VDDD	**O**	**Capacitor**	Internal logic voltage output
VGMP	**O**	**Capacitor**	Reference high voltage for gamma circuit.
VGSP	**O**	**Capacitor**	Reference low voltage for gamma circuit.
VREFP5	**O**	**Capacitor**	Regulator output for VREFP5.
VREFN5	**O**	**Capacitor**	Regulator output for VREFN5.
ELVDD	**O**	**Capacitor**	LDO output used for OLED panel positive voltage. When not in use , please let it open.

ELVSS	**O**	**Capacitor**	LDO output used for OLED panel negative voltage. When not in use , please let it open.
DC/DC pumping			
C11P, C11N **C12P, C12N**	**I/O**	**Charge Pump Capacitor**	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the AVDD voltage. If not used, let them open.
C31P, C31N **C32P, C32N**	**I/O**	**Charge Pump Capacitor**	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VCL voltage. If not used, let them open.
C41P, C41N	**I/O**	**Charge Pump Capacitor**	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage.
C51P, C51N	**I/O**	**Charge Pump Capacitor**	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage.
Other Pins			
PCD_DET	**I**	**VSSD / IOVCC**	Panel break detect pin, When not in use ,please let it open.
T_OTP_RLOAD	**I**	**VSSD / IOVCC**	OTP reload enable. 0: enable OTP reload . 1:disable OTP reload.
T_VBIAS	**O**	**Open**	Test pin, not accessible to user , Must be left open
T_SOURCE	**O**	**Open**	Test pin, not accessible to user , Must be left open
T_VDD2	**O**	**Open**	Test pin, not accessible to user , Must be left open
BSTM	**I**	**Open**	Dummy PAD , leave it open or GND.
TEST1~3	**IO**	**Open**	Test pin, not accessible to user , Must be left open
TESTEN	**I**	**Open**	Test pin, not accessible to user , Must be left open , Internal pull low.
T_EXTCLK	**I**	**Open**	Test pin, not accessible to user , Must be left open
SOUT_DMY1~121	**O**	**Open**	Dummy PAD , Let it open.

6. Interface

6.1. DSI system interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure 7.1 shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.

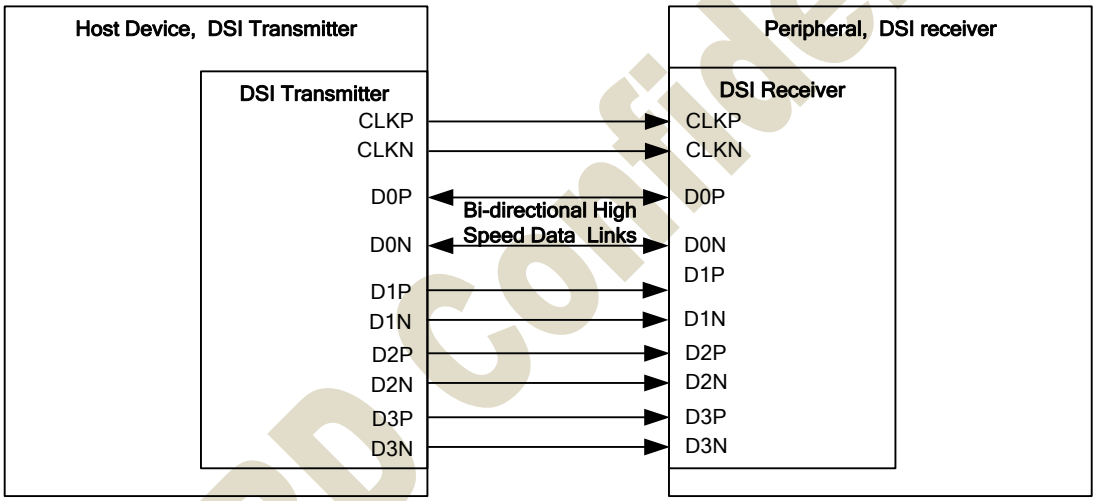


Figure 6.1 DSI transmitter and receiver interface

A conceptual vide of DSI organizes the interface into several functional layers. A description of the layers follows and is also shown in Figure 7.2.

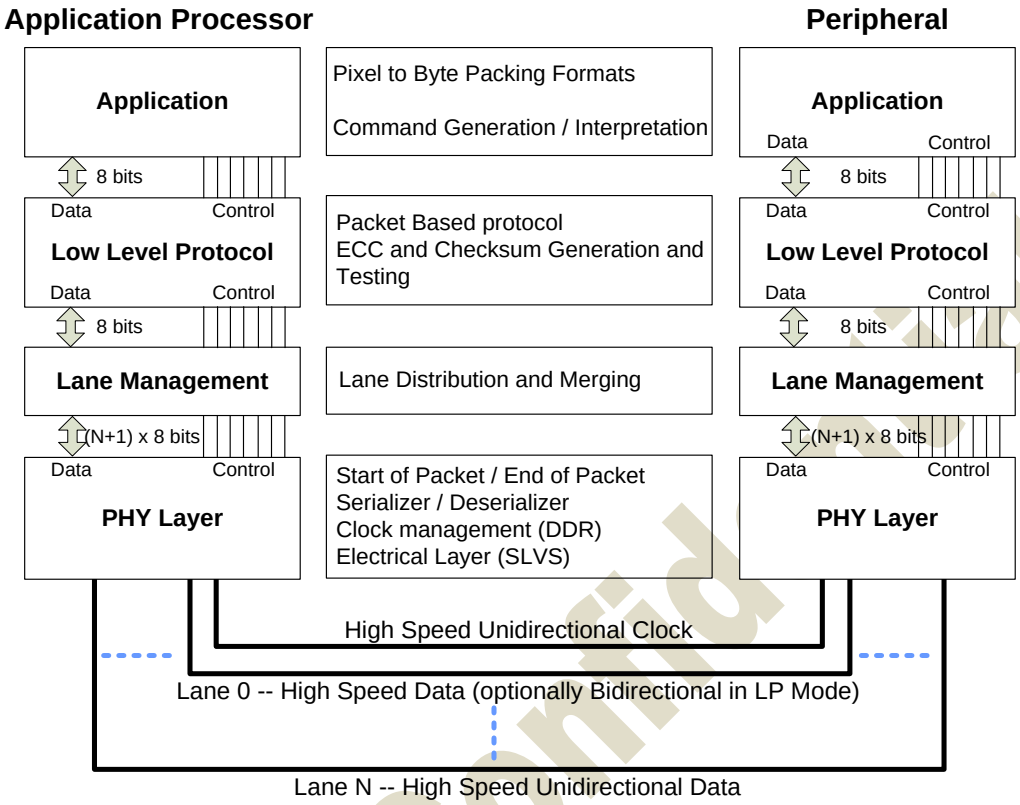


Figure 6.2 DSI Layer

PHY Layer: The PHY Layer specifies transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures “ones” and “zeroes” from the serial bit stream. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

Lane Management Layer: DSI is Lane-scalable for increased performance. The number of data signals may be 1, 2, 3, or 4 depending on the bandwidth requirements of the application. The transmitter side of the interface distributes the outgoing data stream to one or more Lanes (“distributor” function). On the receiving end, the interface collects bytes from the Lanes and merges them together into a recombined data stream that restores the original stream sequence (“merger” function).

Protocol Layer: At the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets. The protocol defines required headers for each packet, and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted.

On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data. DSI protocol also documents how packets may be tagged for interleaving multiple command or data streams to separate destinations using a single DSI.

Application Layer: This layer describes higher-level encoding and interpretation of data contained in the data stream. Depending on the display subsystem architecture, it may consist of pixels having a prescribed format, or of commands that are interpreted by the display controller inside a display module. The DSI specification describes the mapping of pixel values, commands and command parameters to bytes in the packet assembly.

6.1.1. Command mode, Video mode and Virtual Channel

DSI-compliant peripheral support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode

Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode.

Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Virtual Channel Capability

While this specification only addresses the connection of a host processor to a single peripheral, DSI incorporates a virtual channel capability for communication between a

host processor and multiple, physical display modules. Since interface bandwidth is shared between peripherals, there are constraints that limit the physical extent and performance of multiple-peripheral systems. The DSI protocol permits up to four virtual channels, enabling traffic for multiple peripherals to share a common DSI Link. The DSI specification makes no requirements on the specific value assigned to each virtual channel used to designate interlaced fields, For clarity, the first interlaced video field may be assigned as DI[7:6] = 2'b00 and the second interlaced video field may be assigned DI[7:6] = 2'b01.

Note1: JD9613 support both command mode and video mode.

Note2: For JD9613, DI[7:6] for virtual channel should be set as 2’b00.

6.1.2. Power-up Sequence Example

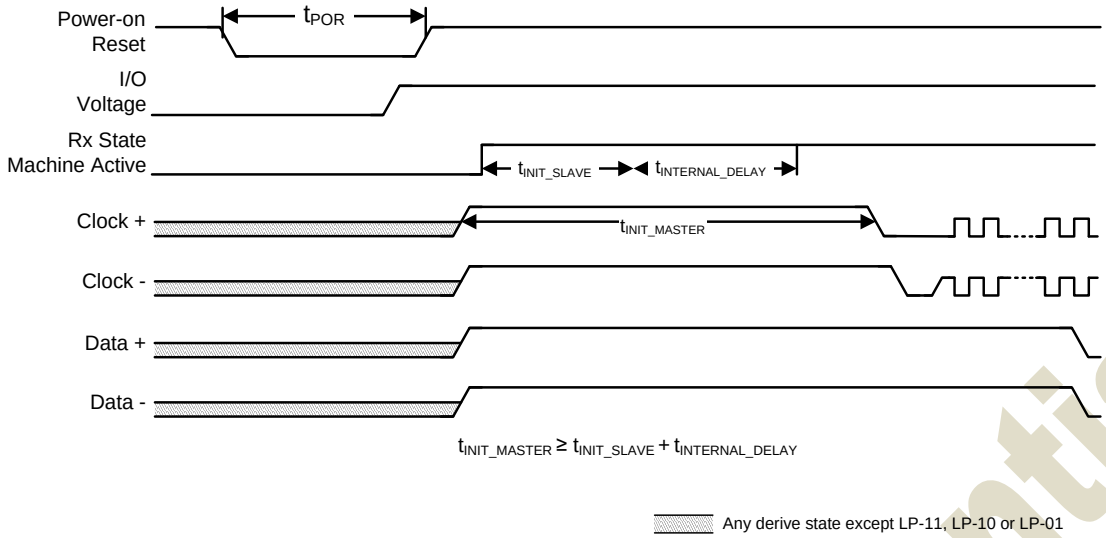


Figure 6.3 Peripheral Power-Up Sequencing Example

6.1.3. DSI Format

Information is transferred between host processor and peripheral using one or more serial data signals and accompanying serial clock. The action of sending high-speed serial data across the bus is called a HS transmission or burst. Between transmissions, the differential data signal or Lane goes to a low-power state (LPS). Interfaces should be in LPS when they are not actively transmitting or receiving high-speed data. Figure 7.4 shows the basic structure of a HS transmission. N is the total number of bytes sent in the transmission

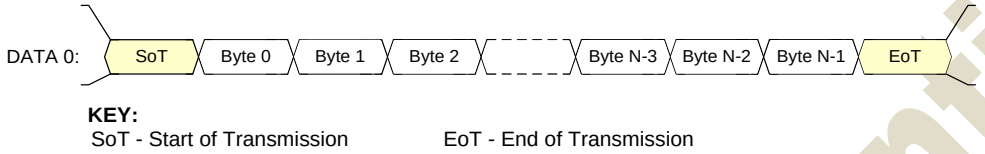


Figure 6.4 Basic HS Transmission Structure

Multi Lane Distribution and Merging

DSI is a Lane-scalable interface. Applications requiring more bandwidth than that provided by one Data Lane may expand the data path to two, three, or four Lanes wide and obtain approximately linear increases in peak bus bandwidth.

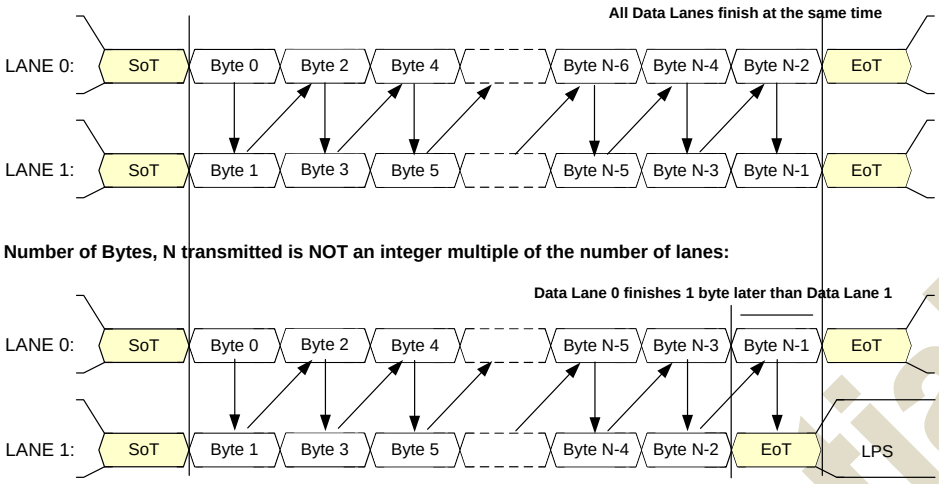
Multi-Lane implementations shall use a single common clock signal, shared by all Data Lanes. Conceptually, between the PHY and higher functional blocks is a layer that enables multi-Lane operation.

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission. Figure 7.5 & 7.6 illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

Number of Bytes, N transmitted is an integer multiple of the number of lanes:

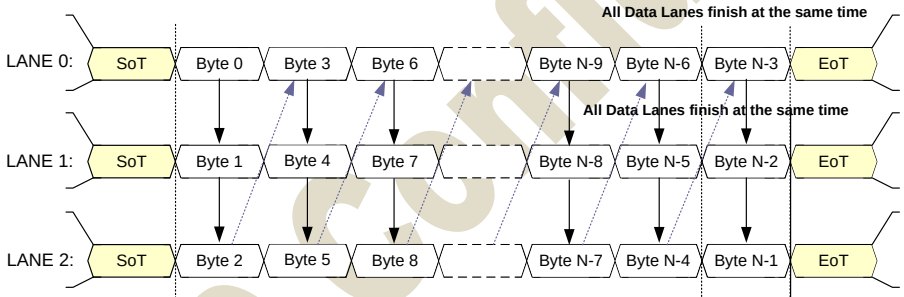


Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes:

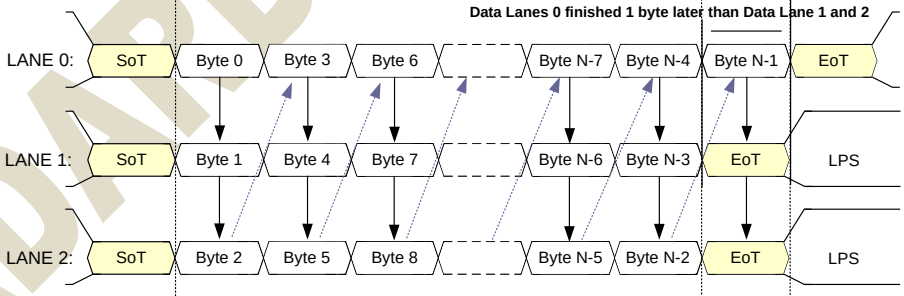
KEY:
LPS - Low Power State SoT - Start of Transmission EoT - End of Transmission

Figure 6.5 Two Lane HS Transmission Example

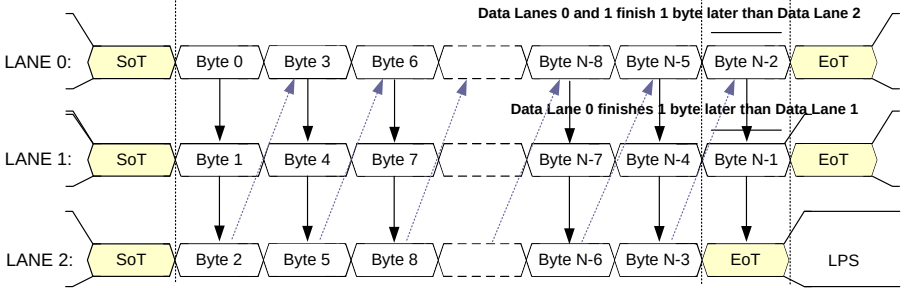
Number of Bytes, N transmitted is an integer multiple of the number of lanes:



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes (Example 1):



Number of Bytes, N transmitted is NOT an integer multiple of the number of lanes (Example 2):



KEY:
LPS - Low Power State SoT - Start of Transmission EoT - End of Transmission

Figure 6.6 Three Lane HS Transmission Example

6.1.4. DSI Protocol

On the transmitter side of a DSI Link, parallel data, signal events, and commands are converted in the Protocol layer to packets, following the packet organization documented in this section. The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY.

6.1.5. Multiple Packets per Transmission

In its simplest form, a transmission may contain one packet. If many packets are to be transmitted, the overhead of frequent switching between LPS and High-Speed Mode will severely limit bandwidth if packets are sent separately, e.g. one packet per transmission.

The DSI protocol permits multiple packets to be concatenated, which substantially boosts effective bandwidth. This is useful for events such as peripheral initialization, where many registers may be loaded with separate write commands at system startup.

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled. The method of enabling or disabling this capability is out of scope for this document.

The top diagram in Figure 7.7 illustrates a case where multiple packets are being sent separately with EoTp support disabled. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets. This constraint does not apply to LP transmissions. The bottom diagram in Figure 7.7 demonstrates a case where multiple packets are concatenated within a single HS transmission.

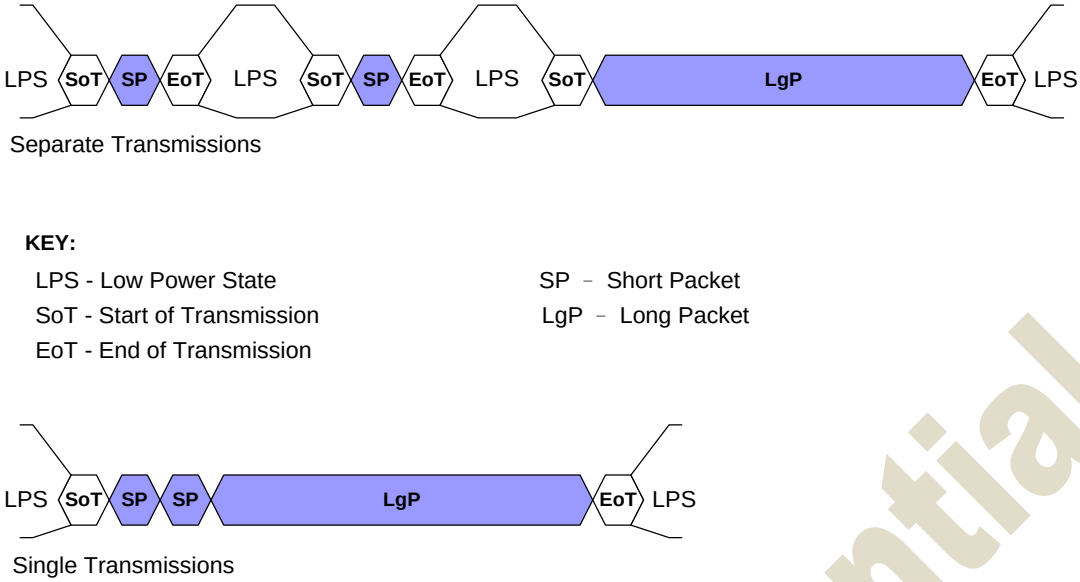


Figure 6.7 HS Transmission Examples with EoTp disabled

Figure 7.8 depicts HS transmission cases where EoTp generation is enabled. In the figure, EoT short packets are highlighted in red. The top diagram illustrates a case where a host is intending to send a short packet followed by a long packet using two separate transmissions. In this case, an additional EoT short packet is generated before each transmission ends. This mechanism provides a more robust environment, at the expense of increased overhead (four extra bytes per transmission) compared to cases where EoTp generation is disabled, i.e. the system only relies on the PHY layer EoT sequence for signaling the end of HS transmission. The overhead imposed by enabling EoTp can be minimized by sending multiple long and short packets within a single transmission as illustrated by the bottom diagram in Figure 7.8.

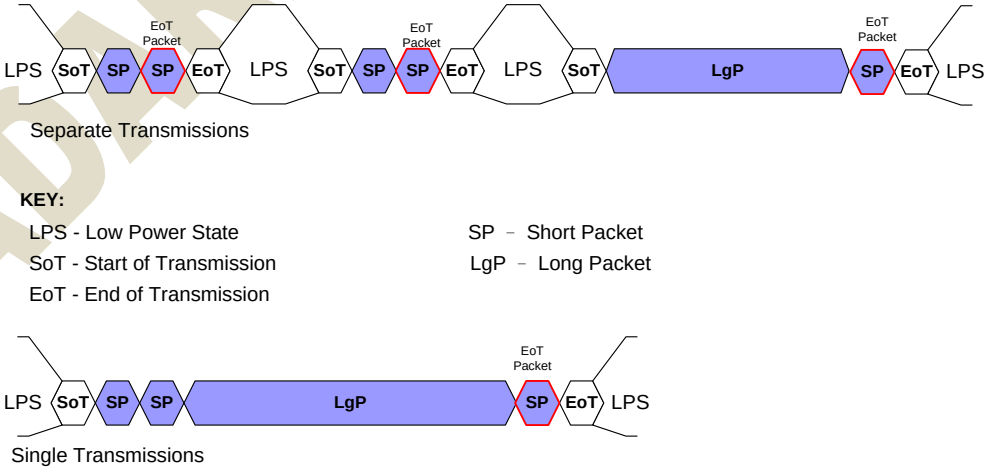


Figure 6.8 HS Transmission Examples with EoTp enabled

6.1.6. Endian Policy

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure 7.9 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

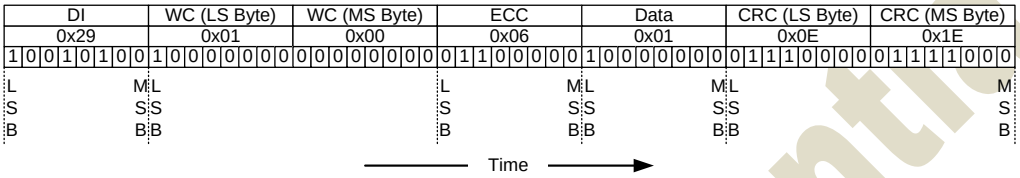


Figure 6.9 Endian Example (Long Packet)

6.1.7. Packet Structure

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Packet sizes fall into two categories:

•**Long packets** specify the payload length using a two-byte Word Count field. Payloads may be from 0 to 216- 1 bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

•**Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

6.1.8. Long Packet

Figure 7.10 shows the structure of the Long packet. A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

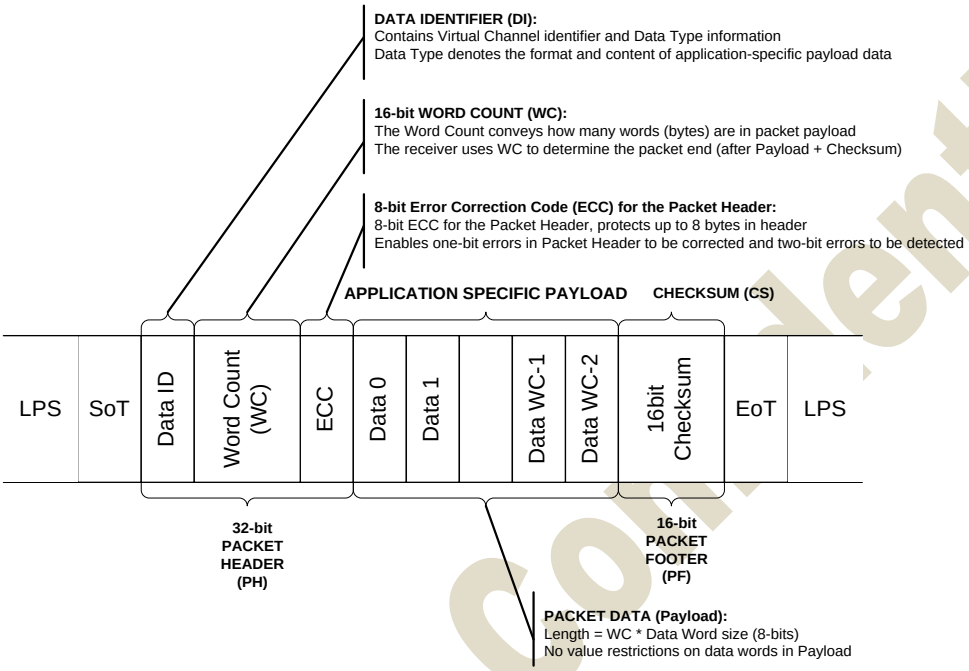


Figure 6.10 Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data.

The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count.

The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields.

After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used.

Once the receiver has read the Data Payload it reads the Checksum in the Packet

Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (0xFFFF). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0x0000). In the generic case, the length of the Data Payload shall be a multiple of bytes.

Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first.

6.1.9. Short Packet

Figure 7.11 shows the structure of the Short packet. A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

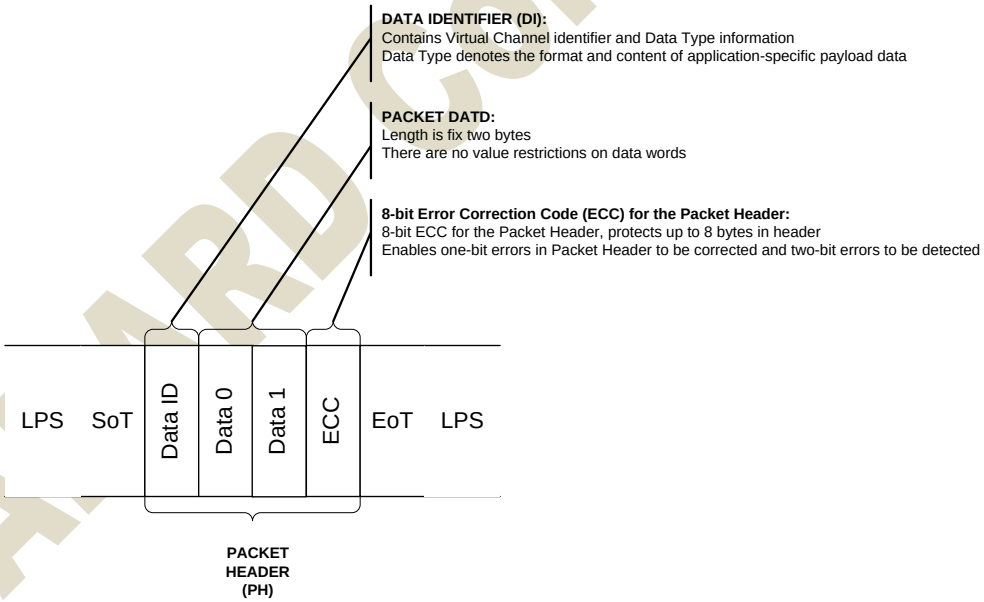


Figure 6.11 Short Packet Structure

6.1.10.Common Packet Elements

Long and Short packets have several common elements that are described in this section.

6.1.11.Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 7.12 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:0]: These six bits specify the Data Type.

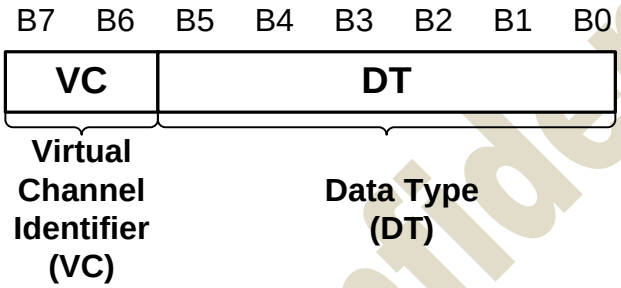


Figure 6.12 Data Identifier Byte

6.1.12.Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel.

6.1.13. Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

6.1.14.ECC

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

6.1.15.DSI packet

6.1.16.Processor-sourced Packets

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 7.1.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x02	00 0010	Color Mode (CM) Off Command	Short
0x12	01 0010	Color Mode (CM) On Command	Short
0x22	10 0010	Shut Down Peripheral Command	Short
0x32	11 0010	Turn On Peripheral Command	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write/write_LUT Command Packet	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xXF unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Table 6.1 Data Types for supported Processor-sourced Packets

6.1.17.Packed Pixel Stream, 16-bit Format, Long Packet

Packed Pixel Stream 16-Bit Format shown in Figure 7.13 is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Within a color component, the LSB is sent first, the MSB last. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

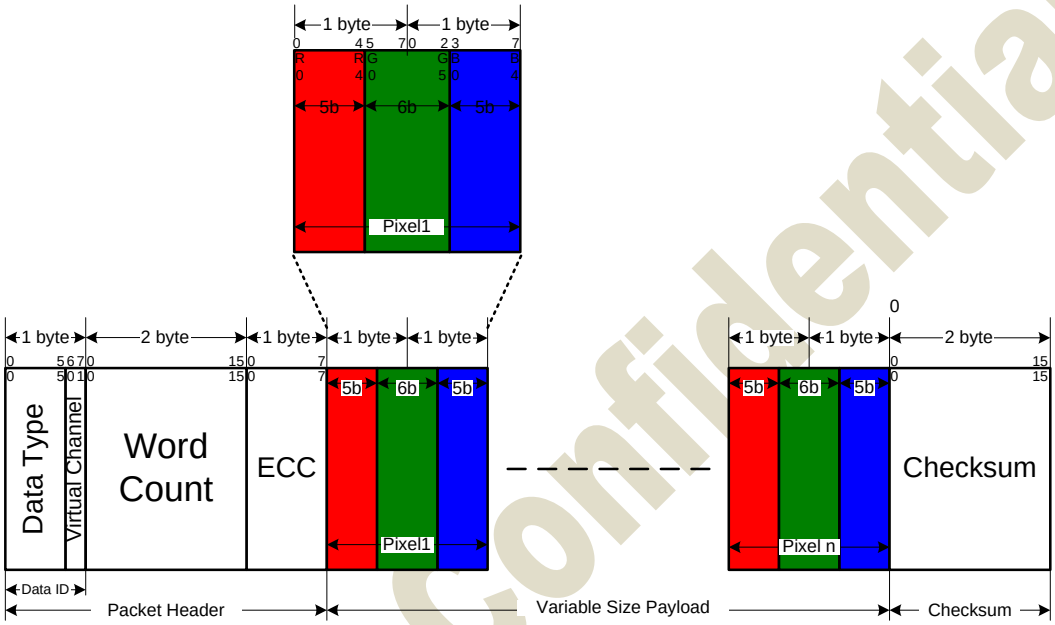


Figure 6.13 16-bit per Pixel – RGB Color Format, Long Packet

6.1.18.Packed Pixel Stream, 18-bit Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) shown in Figure 7.14 is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. Peripheral will not display the fill pixels when refreshing the display device.

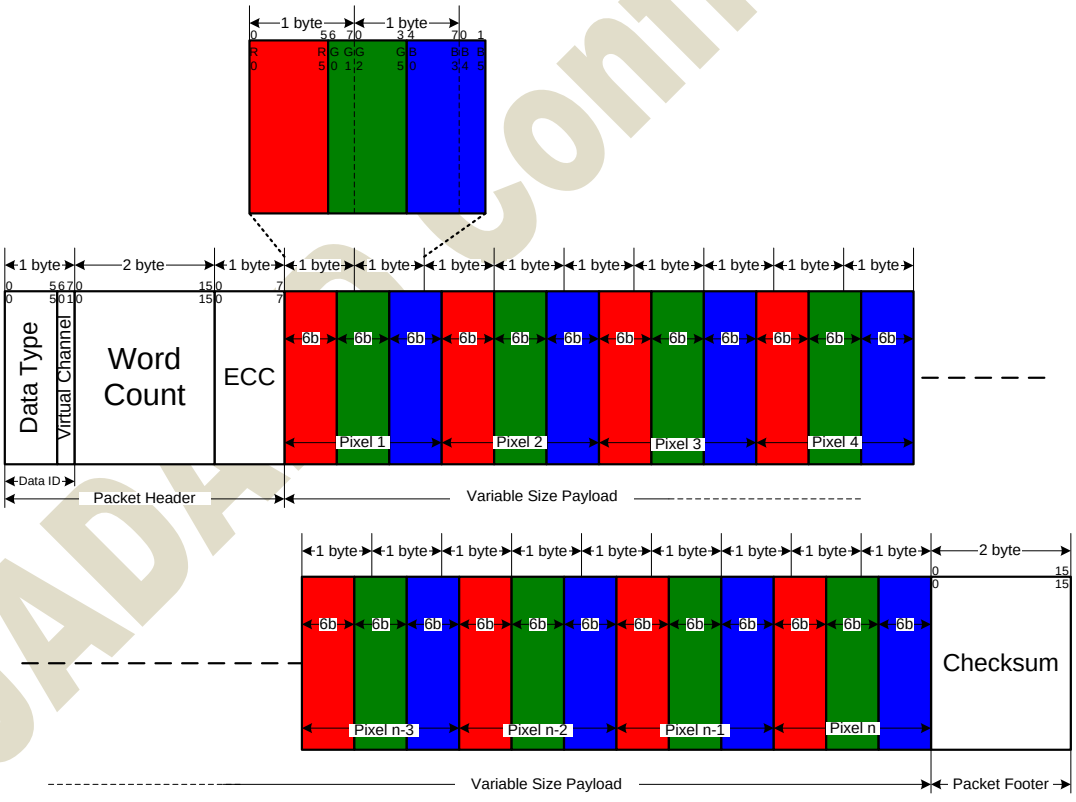


Figure 6.14 18-bit per Pixel (Packed) – RGB Color Format, Long Packet

6.1.19.Pixel Stream, 18-bit Loosely Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits, but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte as shown in Figure 7.15. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

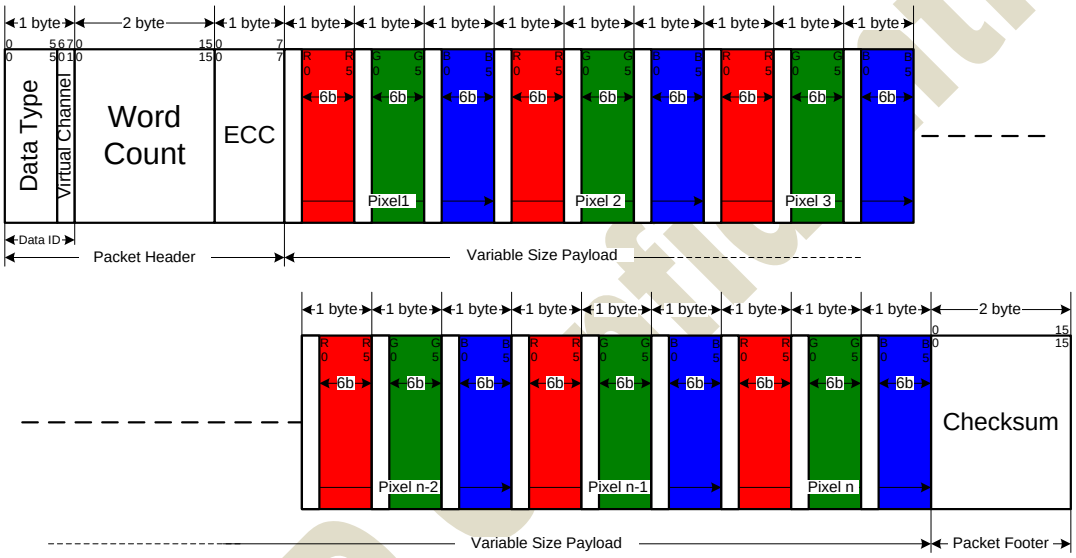


Figure 6.15 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

6.1.20.Packed Pixel Stream, 24-bit Format, Long Packet

Packed Pixel Stream 24-Bit Format shown in Figure 7.16 is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

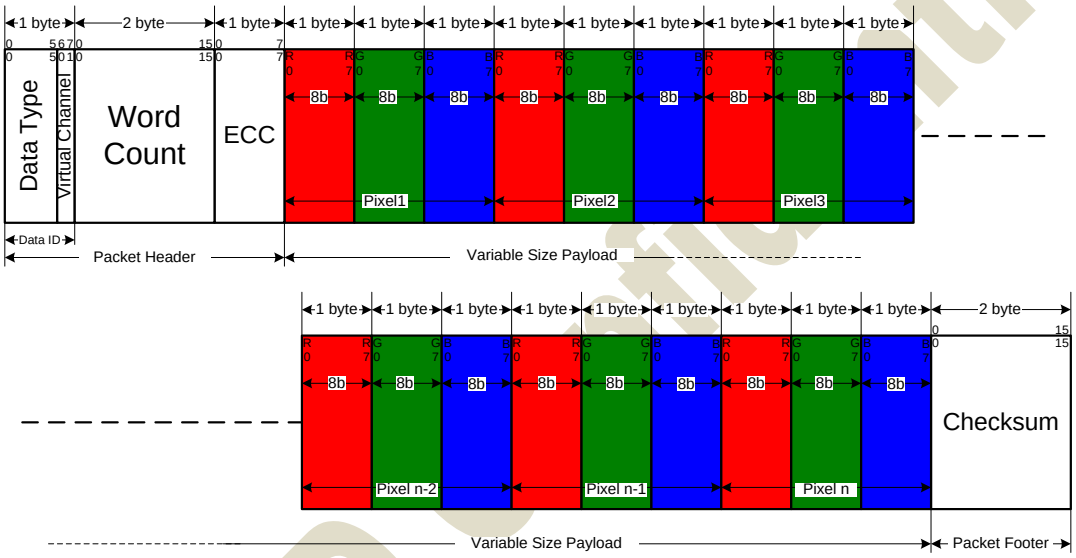


Figure 6.16 24-bit per Pixel – RGB Color Format, Long Packet

6.1.21.Peripheral to Processor Transmission

JD9613 has bidirectional capability for returning READ data, acknowledge, or error information to the host processor. BTA shall take place after every peripheral-to-processor transaction. This returns bus control to the host processor following the completion of the LP transmission from the peripheral. Peripheral-to-processor transactions are of four basic types:

•**Tearing Effect (TE)** is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.

•**Acknowledge** is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, i.e. either triggers or packets, is received by the peripheral with no errors.

•**Acknowledge and Error Report** is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Once reported, accumulated errors in the error register are cleared.

•**Response to Read Request** may be a Short or Long packet that returns data requested by the preceding READ command from the processor.

6.1.22. Appropriate Responses to Commands and ACK Requests

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

•Following a non-Read command, the peripheral shall respond with Acknowledge if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

•Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication, i.e. either triggers or packets.

•Following a Read request if only a single-bit ECC error was detected and corrected, the peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte Acknowledge and Error Report packet in the same LP transmission. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a non-Read command if only a single-bit ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error – Single Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte Acknowledge and Error Report packet without sending Read data. The Error Report shall have the ECC Error – Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte Acknowledge and Error Report packet. The Error Report shall have the ECC Error –

Multi-Bit flag set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

•Following any command, if SoT Error, SoT Sync Error or DSI VC ID Invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge and Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field. Only the Acknowledge and Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

•Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte Acknowledge and Error Report packet with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication. For a read command, only the Acknowledge and Error Report packet shall be transmitted; no read data shall be sent by the peripheral in response.

Once reported to the host processor, all errors documented in this section are cleared from the Error Register.

6.1.23.Peripheral-to-Processor Packet Description

Table7.2 presents the complete set of peripheral-to-processor Data Types.

Data Type (Hex)	Data Type (Binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short
0x08	00 1000	End of Transmission packet	Short
0x1C	01 1100	DCS Long READ Response	Long

Table 6.2 Data Types for Peripheral-sourced Packets

6.1.24.Format of Acknowledge and Error Report and Read Response Data Type

Acknowledge is sent using a Trigger message.

•Byte 0: 00100001 (shown here in first bit [left] to last bit [right] sequence)

Response to Read Request returns data requested by the preceding READ command from the processor. These may be short or Long packets. The format for short READ packet responses is:

•Byte 0: Data Identifier (Virtual Channel ID + Data Type)

•Bytes 1, 2: READ data, may be one or two bytes. For single byte parameters, the parameter shall be returned in Byte 1 and Byte 2 shall be set to 0x00.

•ECC byte covering the header

Acknowledge and Error Report confirms that the preceding command or data sent from the host processor to a peripheral was received, and indicates what types of error were detected on the transmission and any preceding transmissions. Note that if errors accumulate from multiple preceding transmissions, it may be difficult or impossible to identify which transmission contained the error. This message is a Short packet of four bytes, taking the form:

•Byte 0: Data Identifier (Virtual Channel ID + Acknowledge Data Type)

•Byte 1: Error Report bits 0-7

•Byte 2: Error Report bits 8-15

•ECC byte covering the header

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. Table 7.3 shows the bit assignment for all error reporting.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, Single-bit (detected and corrected)
9	ECC Error, Multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Table 6.3 Error Report Bit Definitions

The first eight bits, bit 0 through bit 7, are related to the physical layer errors. Bits 8 and 9 are related to single-bit and multi-bit ECC errors. The remaining bits indicate DSI protocol-specific errors.

6.1.25.Video Mode Interface Timing

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

6.1.26.Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

•**Non-Burst Mode with Sync Pulses –** enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

•**Non-Burst Mode with Sync Events –** similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

•**Burst mode –** RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral.

To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. The host processor should return to LP state once per scanline during the horizontal blanking time.

During the BLLP the DSI Link may do any of the following:

•Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

•Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

•Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

•If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

•Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VSS; all other lines shall start with VSE or HSS. Note that the position of synchronization packets, such as VSS and HSS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet.

Transmission packet components used in the figures in this section are defined in Figure 7.17 unless otherwise specified.

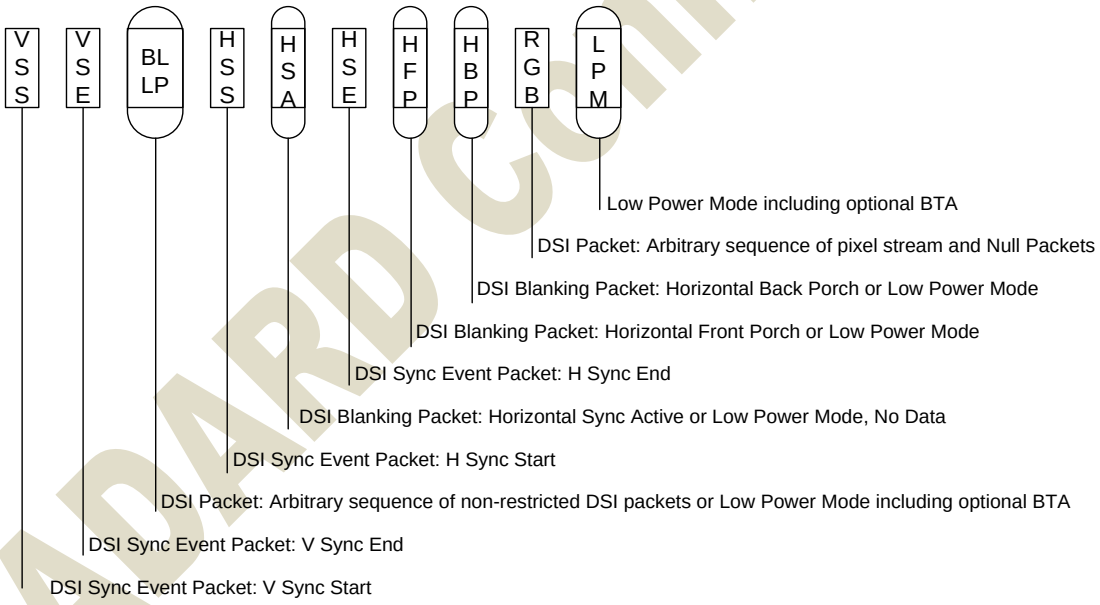


Figure 6.17 Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

6.1.27.Non-Burst sync pulse mode

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure 7.18.

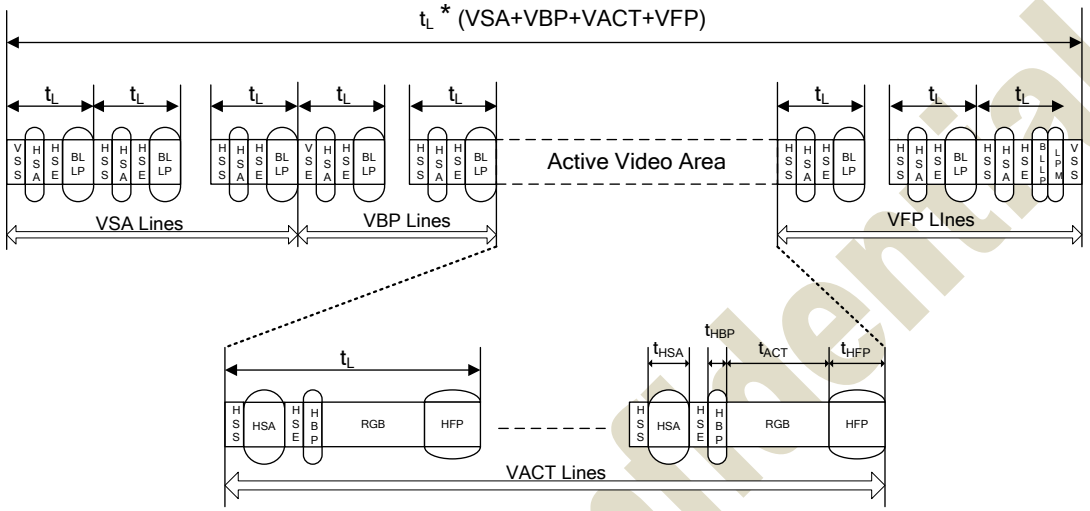


Figure 6.18 Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power. During HSA, HBP and HFP periods, the bus should stay in the LP-11 state.

6.1.28.Non-Burst sync event mode

This mode is a simplification of the “Non-Burst Mode with Sync Pulses” format. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. An example of this mode is shown in Figure 7.19.

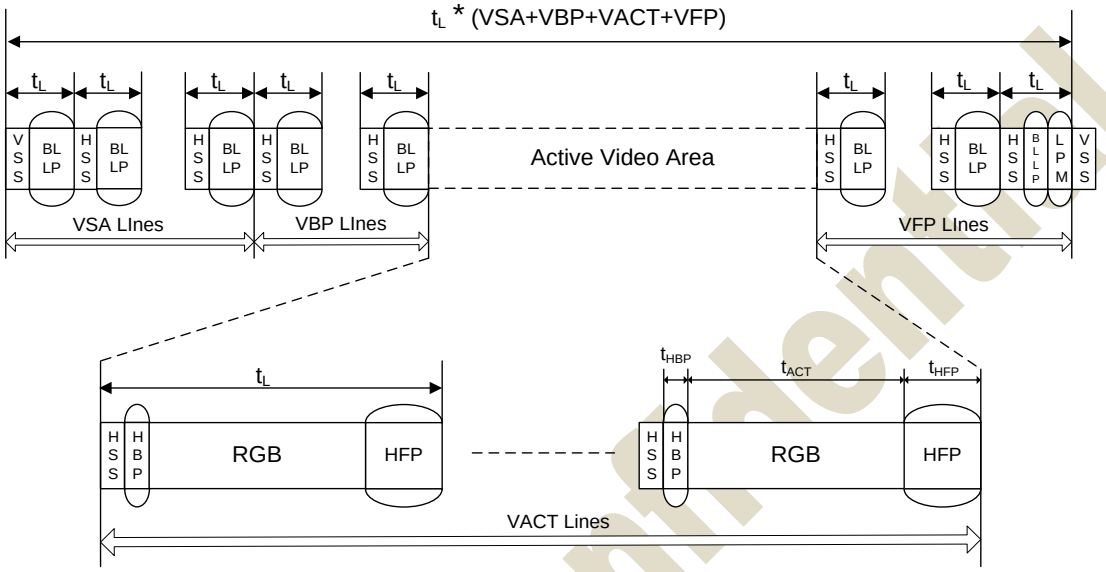


Figure 6.19 Video Mode Interface Timing: Non-burst Transmission with Sync Events

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

6.1.29.Burst mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction.

Following HS pixel data transmission, the bus may stay in HS Mode for sending blanking packets or go to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure 7.20.

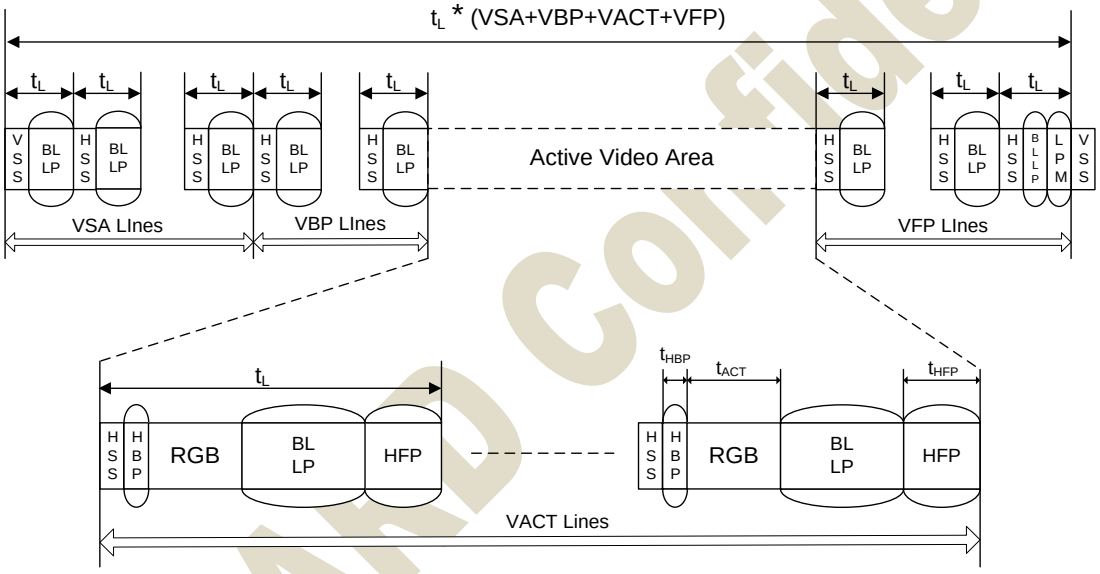


Figure 6.20 Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

6.1.30.Error-Correcting Code and Checksum

6.1.31.Error-Correcting Code(ECC)

MIPI DSI uses Hamming Code Theory as ECC generate rule. The parity of each bits in ECC are showed as below.

P7=0

P6=0

P5=D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4=D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3=D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2=D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1=D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0=D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC is generated from the twenty-four bits with in the Packet Header as illustrated in Figure 7.21, which also serves as an ECC calculation example.

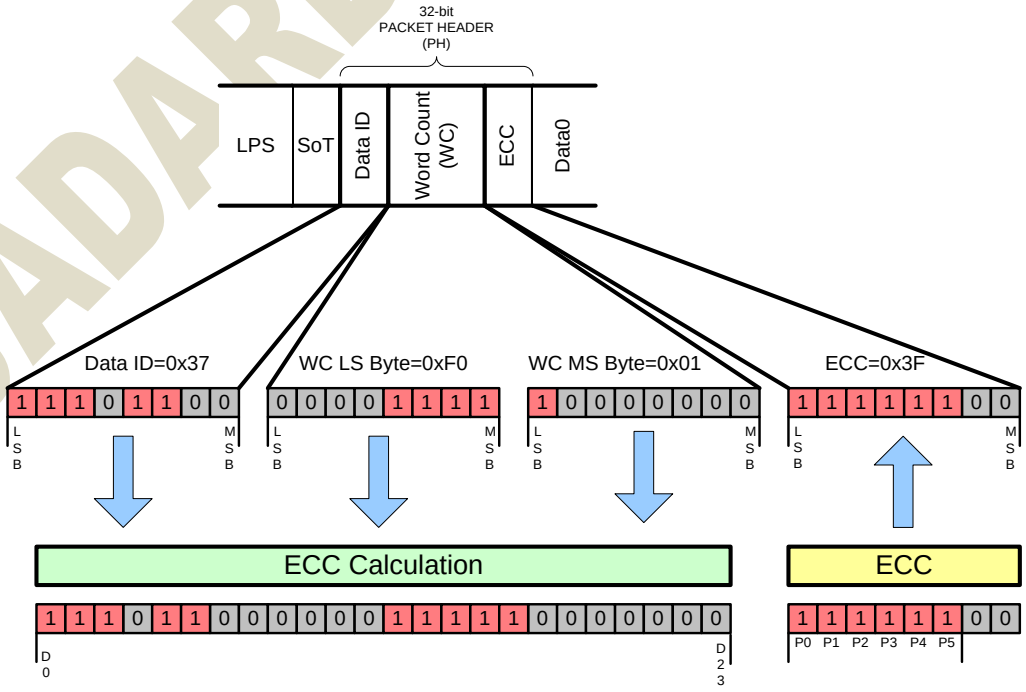


Figure 6.21 24-bit ECC generation Example

6.1.32.Checksum Generation for Long Packet Payloads

To detect errors in transmission of Long packets, a checksum is calculated over the payload portion of the data packet. Note that, for the special case of a zero- length payload, the 2-byte checksum is set to 0xFFFF. The checksum shall be realized as a 16-bit CRC with a generator polynomial of x^16+x^12+x^5+x^0

The transmission of the checksum is illustrated in Figure 7.22. The LS byte is sent first, followed by the MS byte. Note that within the byte, the LS bit is sent first.

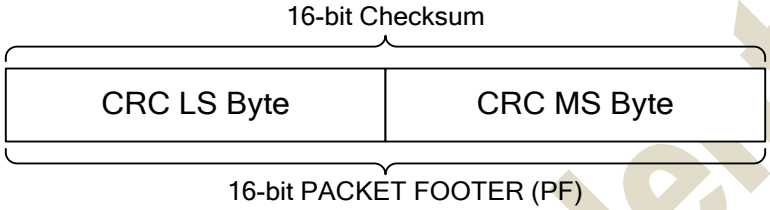


Figure 6.22 Checksum Transmission

The CRC implementation is presented in Figure 7.23. The CRC shift register shall be initialized to 0xFFFF before packet data enters. Packet data not including the Packet Header then enters as a bitwise data stream from the left, LS bit first. Each bit is fed through the CRC shift register before it is passed to the output for transmission to the peripheral. After all bytes in the packet payload have passed through the CRC shift register, the shift register contains the checksum. C15 contains the checksum's MSB and C0 the LSB of the 16-bit checksum. The checksum is then appended to the data stream and sent to the receiver. The receiver uses its own generated CRC to verify that no errors have occurred in transmission.

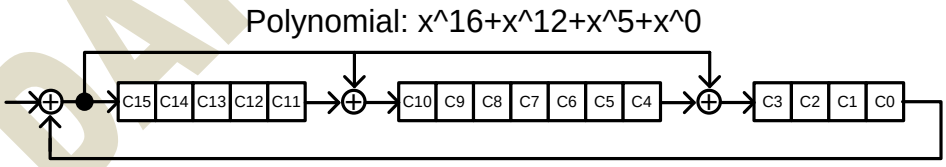


Figure 6.23 16-bit CRC Generation Using a Shift Register

6.1.33.DPHY

6.1.34.Lane Module

A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect wires simultaneously, one or more single-ended Low-Power functions operating on each of the interconnect wires individually, and control & interface logic. For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has to be matched.

6.1.35.Lane Module Type of Clock Lane, Data0, Data1 and Data2

The required functions in a Lane Module depend on the Lane type and which side (master or slave) of the Lane Interconnect the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. In JD9613 Below show the lane module architecture of each lane.

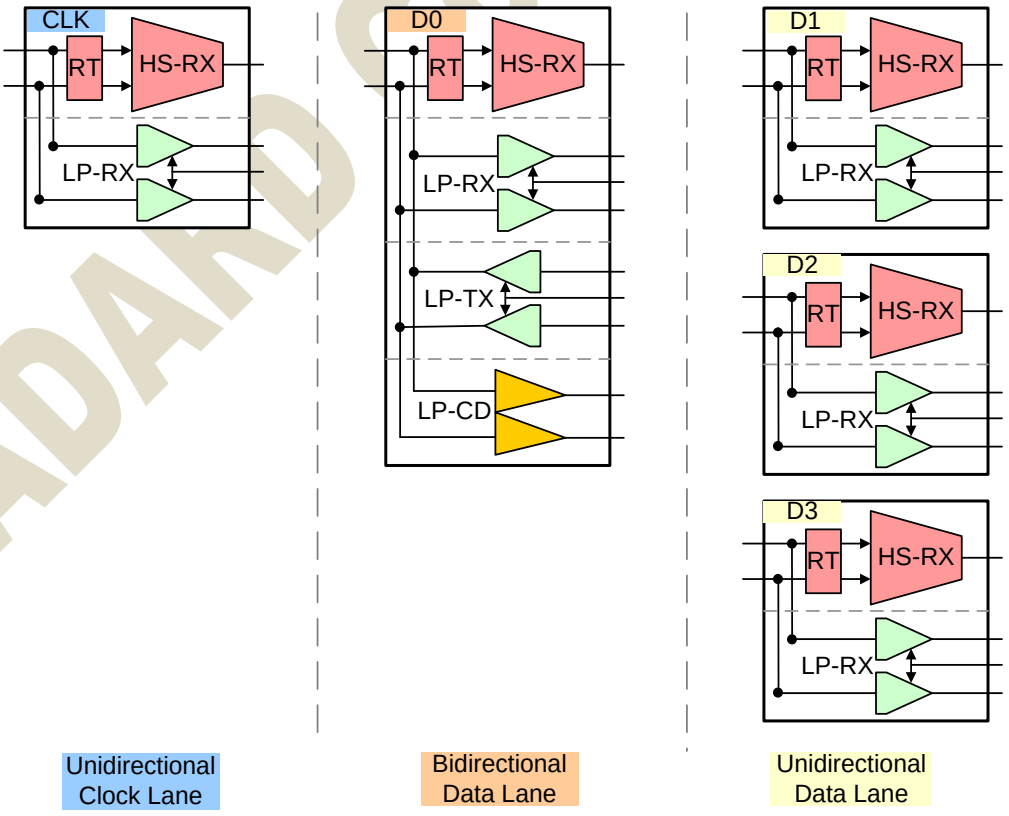


Figure 6.24 Lane Module Type

6.1.36.Master and Slave

Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. The main direction of data communication, from source to sink, is denoted as the Forward direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

JD9613 serves as Slave side.

6.1.37.Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line levels. During normal operation either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High- Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential- 0 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The LP-Receivers shall always interpret both High-Speed differential states as LP-00.

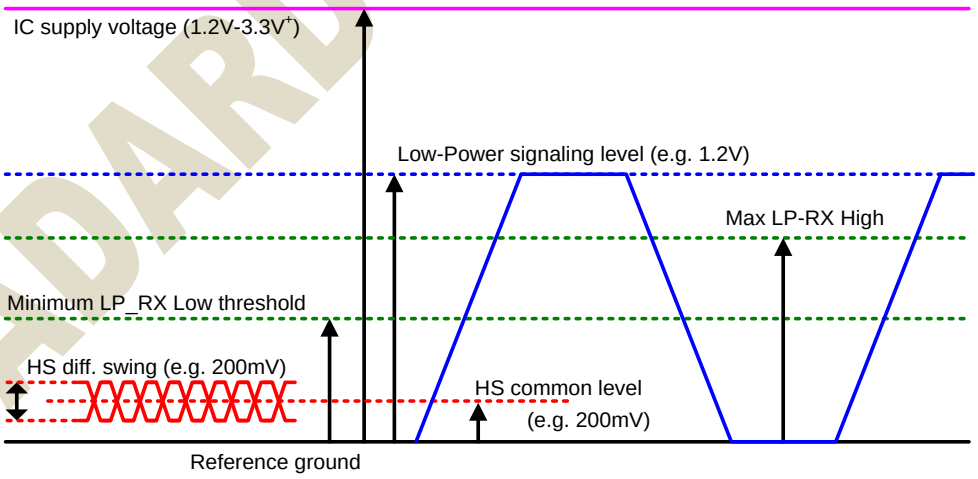


Figure 6.25 Line Levels

The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 7.4 lists all the states that can appear on a Lane

during normal operation. All LP state periods shall be at least TLPX in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the reconstructed clock has a duration of at least 2*TLPX, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Start Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

Table 6.4 Lane State Descriptions

6.1.38.Bi-directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. Notice that Master and Slave side shall not be changed by Turnaround.

Figure 7.26 shows the Turnaround procedure graphically.

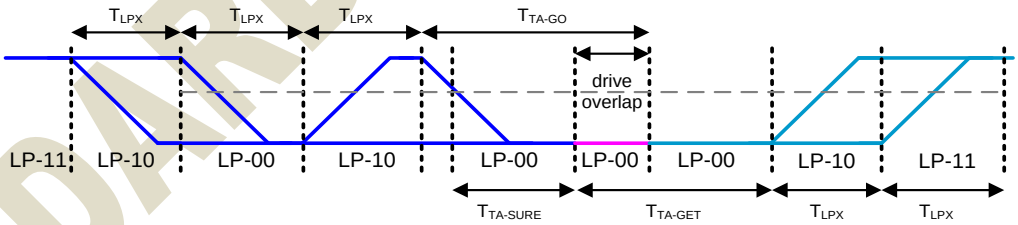


Figure 6.26 Turnaround Procedure

6.1.39.Escape Mode

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command, by Spaced-One-Hot coding, to indicate the requested action. Table 7.5 lists all supported Escape mode commands and actions.

Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0 followed by a Space to transmit a ‘zero-bit’ and it shall send a Mark-1 followed by a Space to transmit a ‘one-bit’. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a Space state.

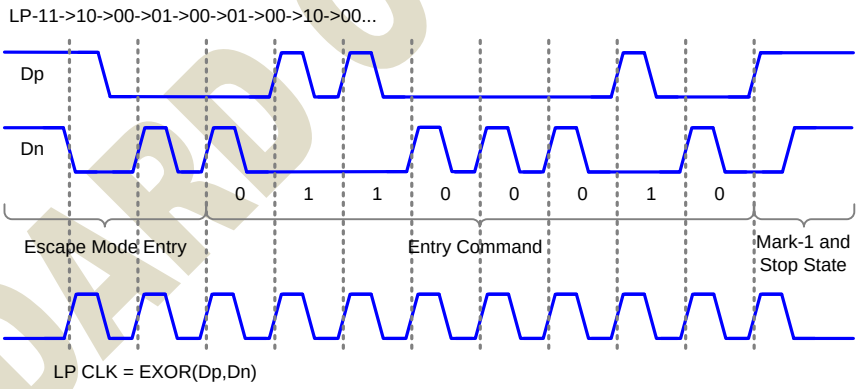


Figure 6.27 Trigger-Reset Command in Escape Mode

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low power State	mode	00011110
Reset-Trigger	Trigger	01100010
TE-Trigger	Trigger	01011101
Acknowledge	Trigger	00100001

Table 6.5 Escape Entry Codes

6.1.40.Remote Trigger

Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode capability and at least one matching Trigger Escape Entry Command on both sides of the interface. Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

6.1.41.Low-Power Data Transmission(LPDT)

If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in Low-Power mode. Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands. The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT, exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. At the end of LPDT the Lane shall return to the Stop state.

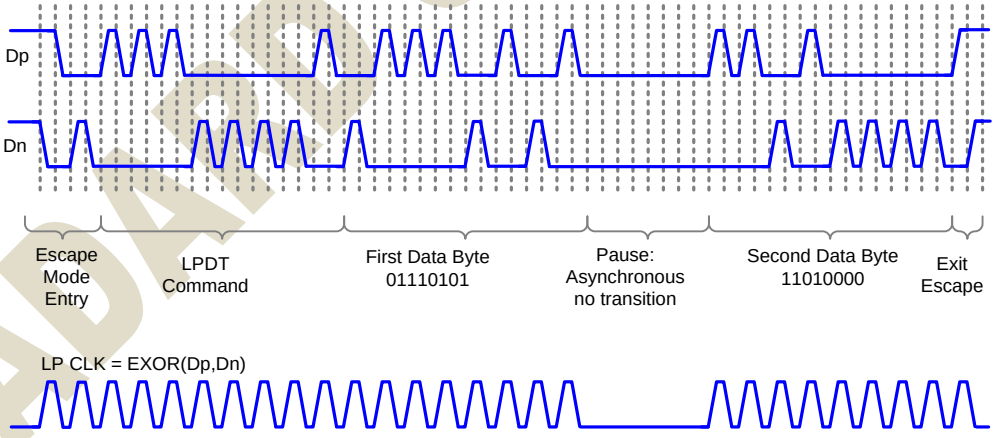


Figure 6.28 Two Data Byte Low-Power Data Transmission Example

6.1.42.Ultra-Low Power State(ULPS)

If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

6.1.43.TE Trigger

A Command Mode display module has its own timing controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bidirectional Data Lane.

For polling to the display module, the host processor shall detect the current scan line information with a DCS command such as get_scan_line to avoid Tearing Effects. For TE-reporting from the display module, the TE-reporting function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_scanline, and set_tear_off.

set_tear_on and set_tear_scanline are sent to the display module as DSI Data Type 0x15 (DCS Short Write, one parameter) and DSI Data Type 0x39 (DCS Long Write/write_LUT), respectively. The host processor ends the transmission with Bus Turn-Around asserted, giving bus possession to the display module. Since the display module's DSI Protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with a normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession.

To enable TE-reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE reporting has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) Bus Turn-Around signal to its D-PHY functional block. The PHY layer will then initiate a Bus Turn-Around sequence in LP mode, which gives bus possession to

the display module.

Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait for up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or requests to the display module, because it does not have bus possession.

When the TE event takes place the display module shall send TE event information in LP mode using a specified trigger message available with D-PHY protocol via the following sequence:

•The display module shall send the LP Escape Mode sequence

•The display module shall then send the trigger message byte 01011101 (shown here in first bit to last bit sequence)

•The display module shall then return bus possession to the host processor

This Trigger Message is reserved by DSI for TE signaling only and shall not be used for any other purpose in a DSI-compliant interface.

6.1.44.High Speed Transmission

6.1.45.Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data bytes with a minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of bytes implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the best choice is for maximum burst length.

6.1.46.Start-of-Transmission

After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of a Start-of-Transmission (SoT) procedure. Table 7.6 describes the sequence of events on TX and RX side.

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS-PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D-TERM-EN}$
Enables High-Speed driver and disables Low-Powerdrivers simultaneously.	
Drives HS-0 for a time $T_{HS-ZERO}$	Enables HS-RX and waits for timer $T_{HS-SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence ‘00011101’ beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence ‘011101’
Continues to Transmit High-Speed payload data	
	Receives payload data

Table 6.6 Start-of-Transmission Sequence

6.1.47.End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 7.7 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS-SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

Table 6.7 End-of-Transmission Sequence

6.1.48.High Speed Data Transmission

Figure 7.29 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane.

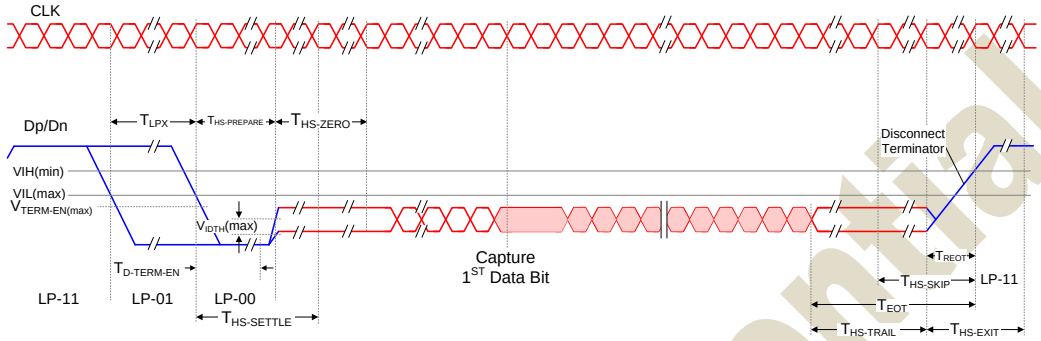


Figure 6.29 High-Speed Data Transmission in Bursts

6.1.49.High Speed Clock Transmission

In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of the first transmitted bit of a burst. The detail Clock Start and Stop procedures are shown in Figure 7.30.

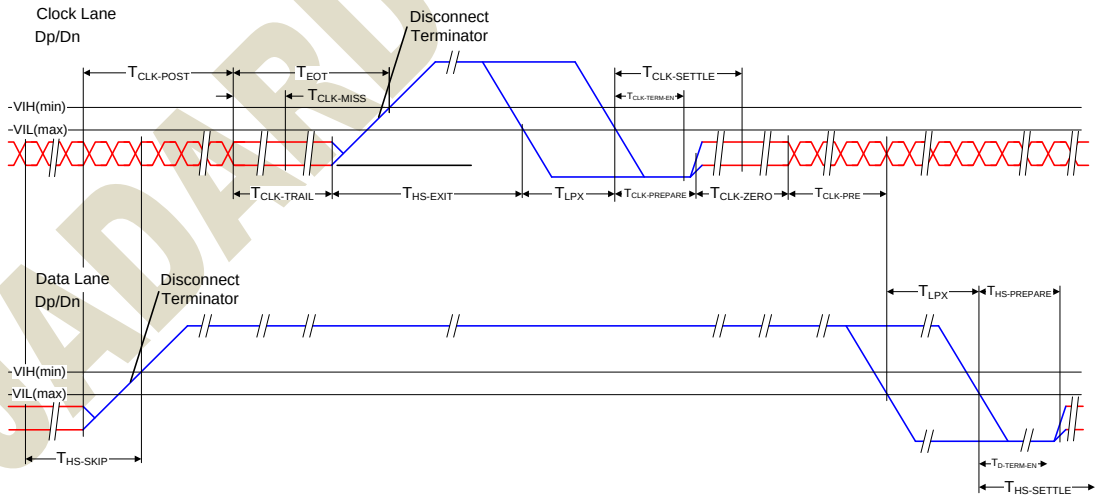


Figure 6.30 Switching the Clock Lane between Clock Transmission and Low-Power Mode

6.1.50.System Power state

Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State.

6.1.51.Initialization

After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer then TINIT. The first Stop state longer than the specified TINIT is called the Initialization period. The Master side shall ensure that a Stop State longer than TINIT does not occur on the Lines before the Master is initialized.

TINIT must larger than 500us.

6.1.52.Global Operation Flow Diagram

Figure 7.31 shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround, and Initialization.

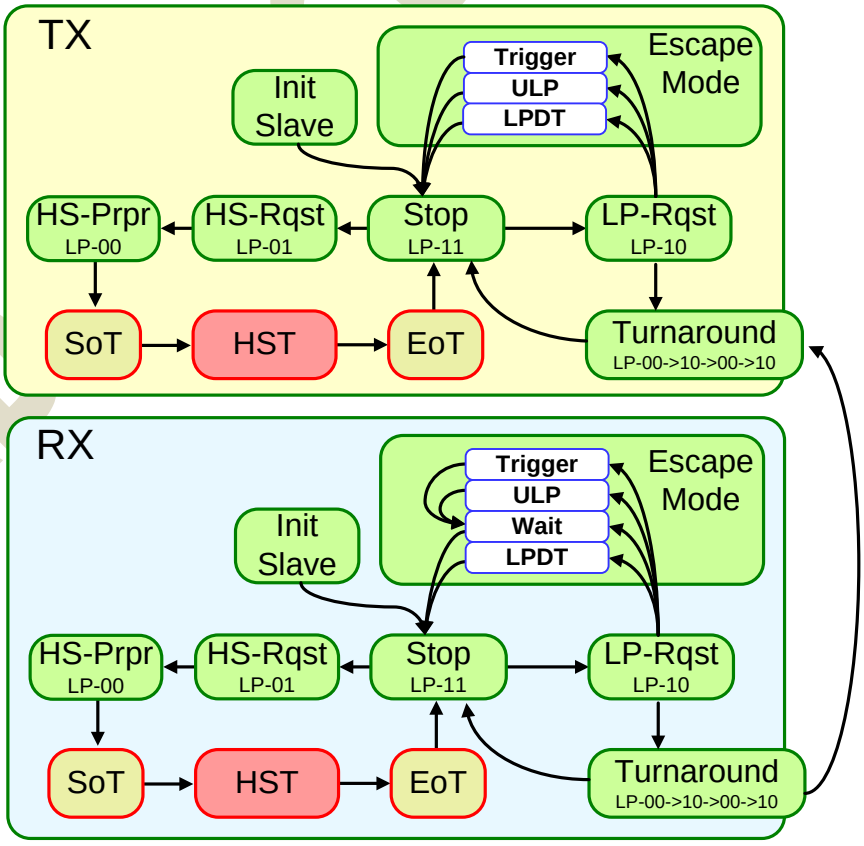


Figure 6.31 Data Lane Module State Diagram

Figure 7.32 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High- Speed clock transmission.

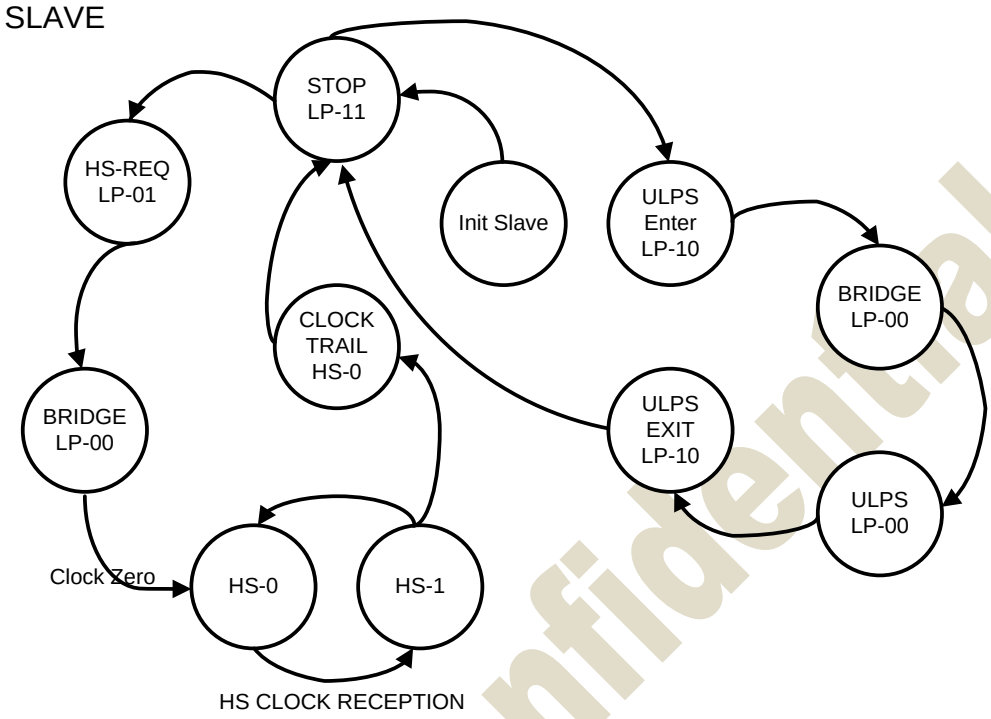


Figure 6.32 Clock Lane Module State Diagram

6.2. MPU system interface

JD9613 provides the 8-bit parallel system interface for 8080-I series, and 3-/4-line /Quad serial system interface for serial data input . The input system interface is selected by external pins IM[1:0] and the bit formal per pixel color order is selected by COLMOD(3Ah) register.

6.2.1. MCU interface selection

The selection of interface is done by setting external pins IM [1:0] as shown in the following table.

IM1	IM0	Command / Display Data	Data Pin
0	0	MIPI	HS_CKP/N, D0P/N, D1P/N
		3-wire SPI	SDI_RDX, SDO
0	1	MIPI	HS_CKP/N, D0P/N, D1P/N
		4-wire SPI	SDI_RDX, SDO
1	0	MIPI	HS_CKP/N, D0P/N, D1P/N
		Quad SPI	SDI_RDX, SDO, DCX, DB[1:0]
1	1	MCU 8bits	DB[7:0]

If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together.

6.2.2. 8080-I Series Parallel Interface

JD9613 can be accessed via 8bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable JD9613 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[7:0] is parallel data bus.

JD9613 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [7:0] bits are display RAM data or command's parameters. When D/CX='0', D[7:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and AMOLED driver chip. The 8080-I Interface selection is done when IM[1:0] pin is high state (IOVCC level).

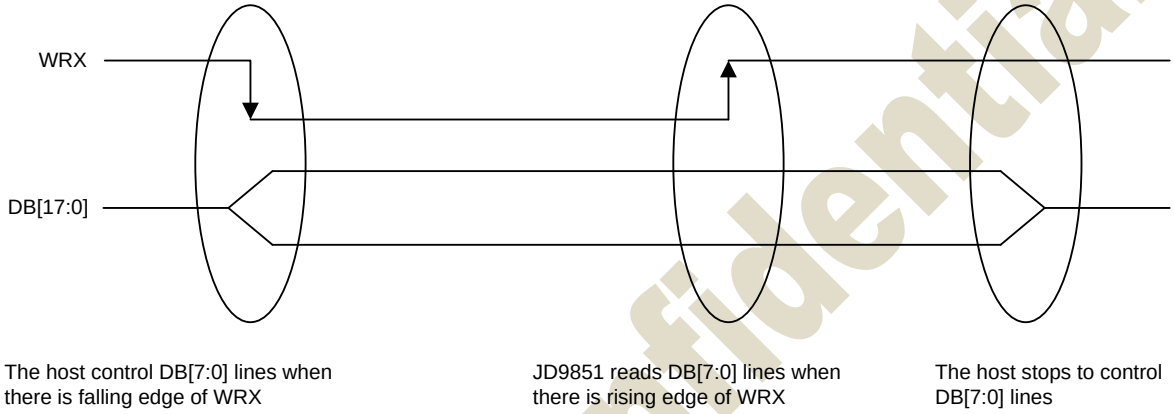
The selection of 8080-I series parallel interface is shown as the table in the following.

IM1	IM0	Interface	CSX	D/CX	RDX	WRX	Function
1	1	8-bit parallel	0	0	1	↑	Write 8-bit command (DB[7:0])
			0	1	1	↑	Write 8-bit display data or 8-bit parameter (DB[7:0])
			0	1	↑	1	Read 8-bit display data (DB[7:0])
			0	1	↑	1	Read 8-bit parameter or status (DB[7:0])

6.2.2.1. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is GRAM data or command's parameter.

The following figure shows a write cycle for the 8080-I MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 6.33 8080-I Series WRX Protocol

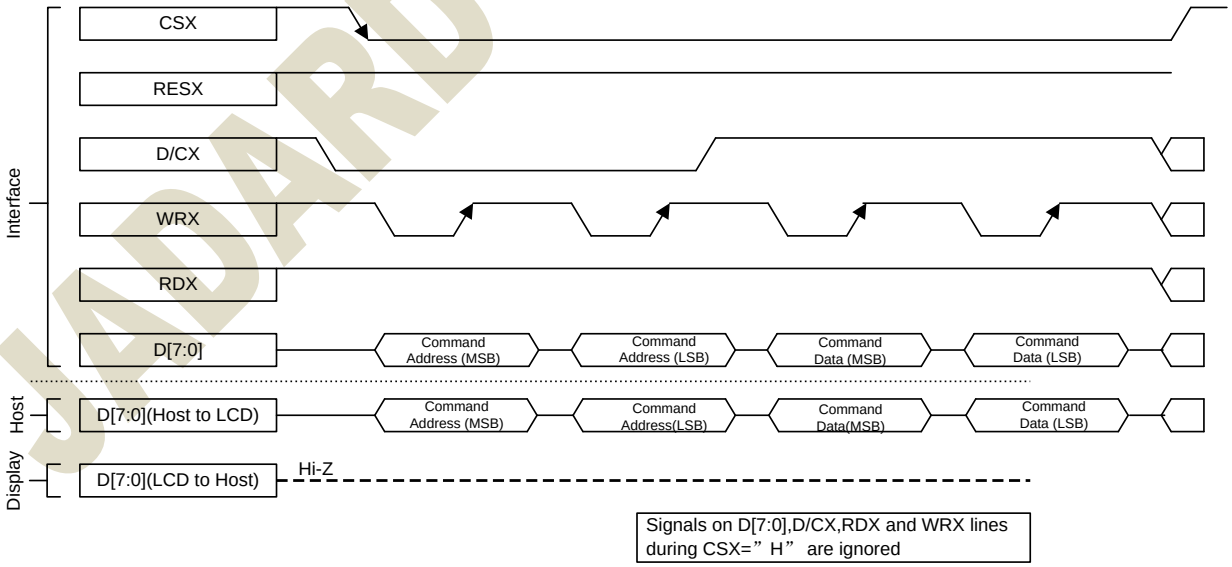
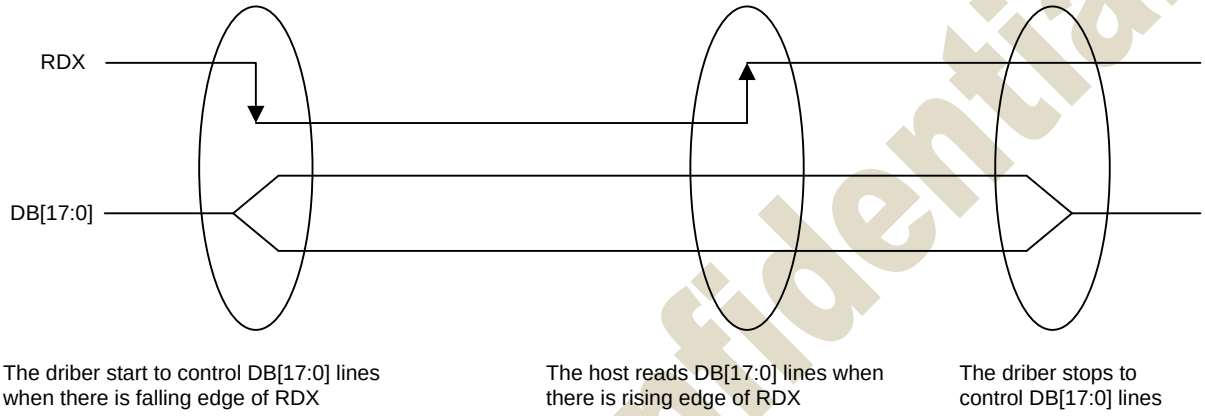


Figure 6.34 8080-I Series Parallel Bus Protocol, Write Register or Display RAM

6.2.2.2. Read Cycle Sequence

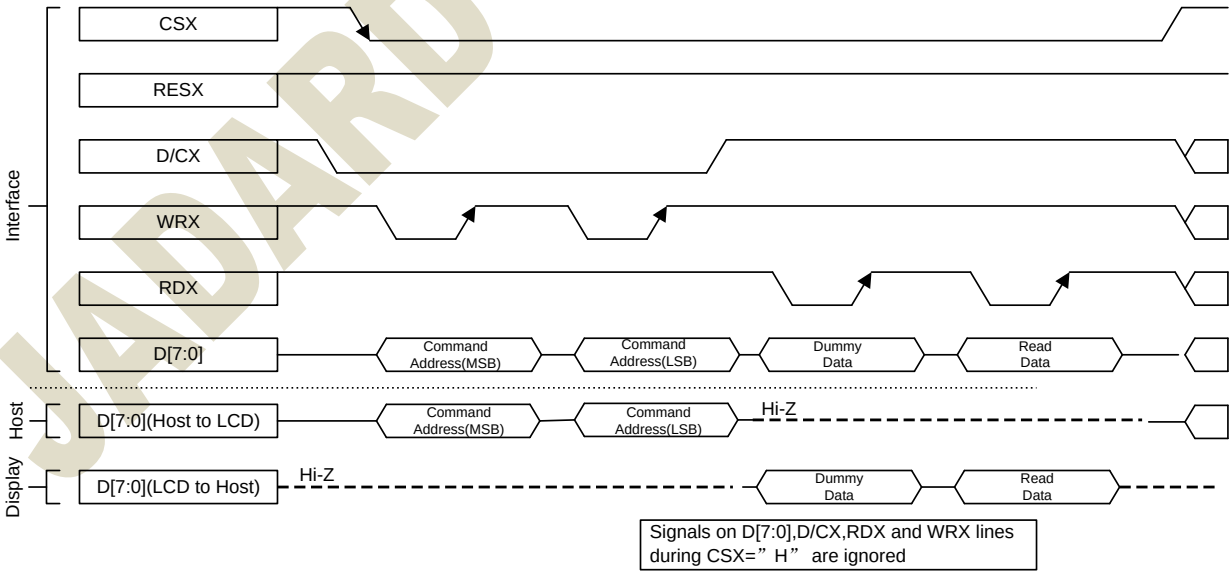
The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-I MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped)

Figure 6.35 8080-I Series RDX Protocol



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

Figure 6.36 8080-I Series Parallel Bus Protocol, Read Register or Display RAM

6.2.3. Serial Interface

The selection of interface is done by IM [1:0] bits. Please refer to the Table in the following.

IM1	IM0	MCU-Interface Mode	Read back selection
0	0	3-line serial interface	Via the read instruction
0	1	4-line serial interface	
1	0	Quad serial interface	

JD9613 supplies 3-lines and 4-line and Quad serial interfaces for communication between host and JD9613. The Quad serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDI_RDX), input(DCX,DB[0],DB[1]). The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input (SDI_RDX) and serial data output (SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input(SDI_RDX) and Output (SDO) for data transmission. The data bus (D [7:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary. If the host places the SDI_RDX line into high-impedance state during the read interval, the SDI_RDX and SDO can be tied together.

6.2.3.1. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to JD9613. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to JD9613 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

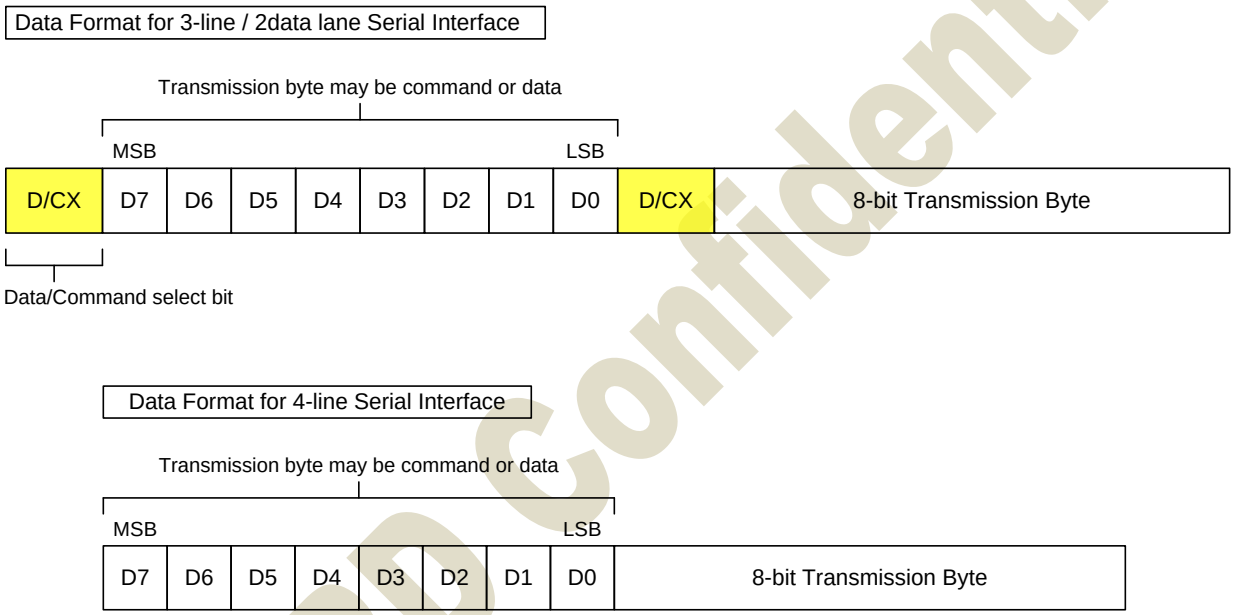
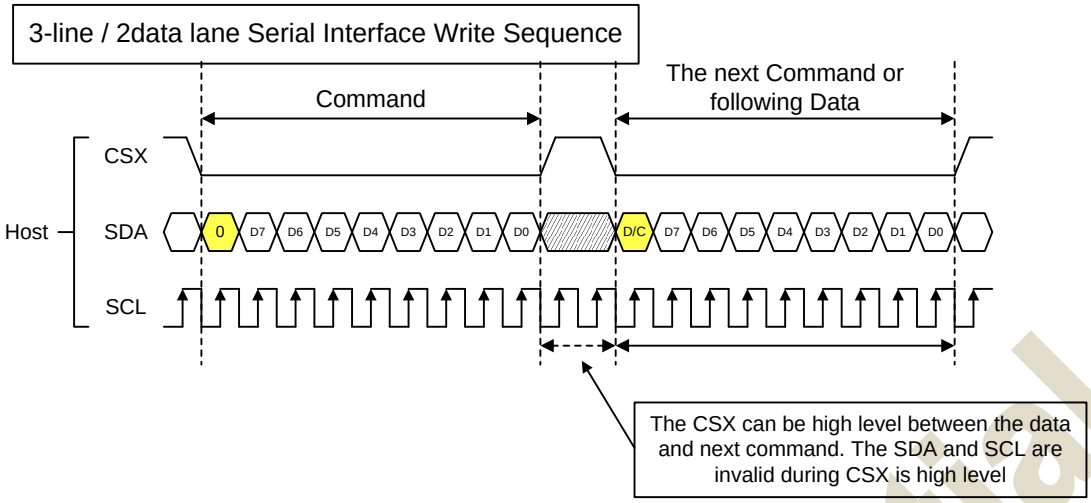


Figure 6.37 Serial interface data stream format

Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by JD9613 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



Note: Enter 2 data lane interface the register DSPI_EN=1 and DSPI_CFG[1:0]=01 / 10 / 11

Figure 6.38 3-line / 2data lane serial interface write protocol

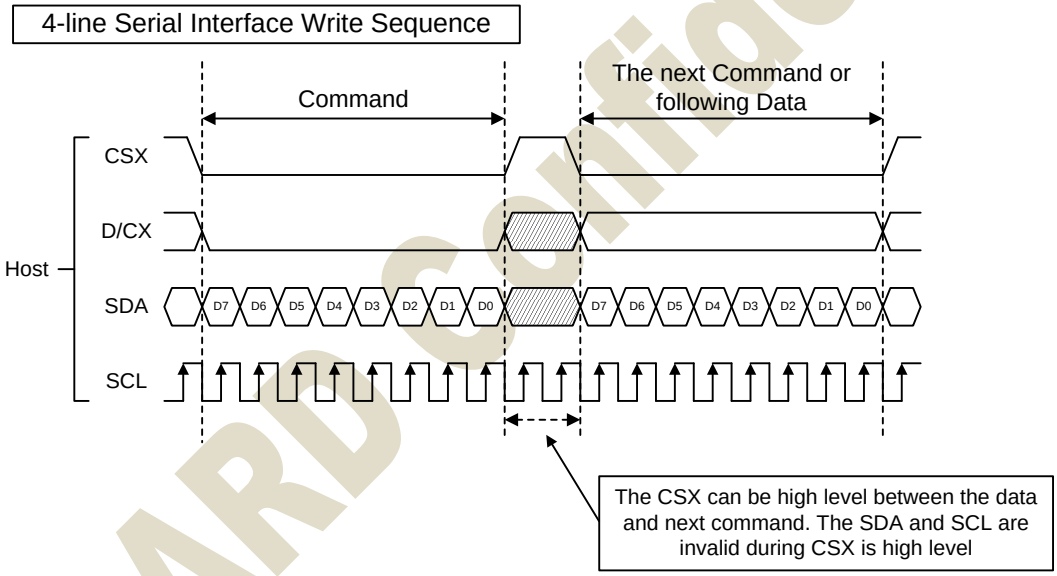


Figure 6.39 4-line serial interface write protocol

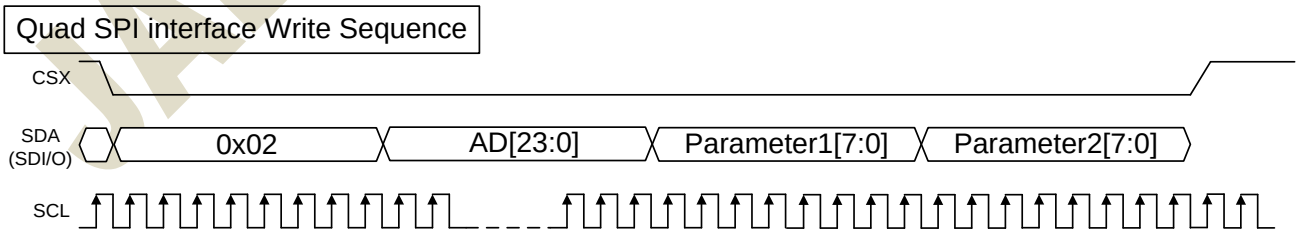
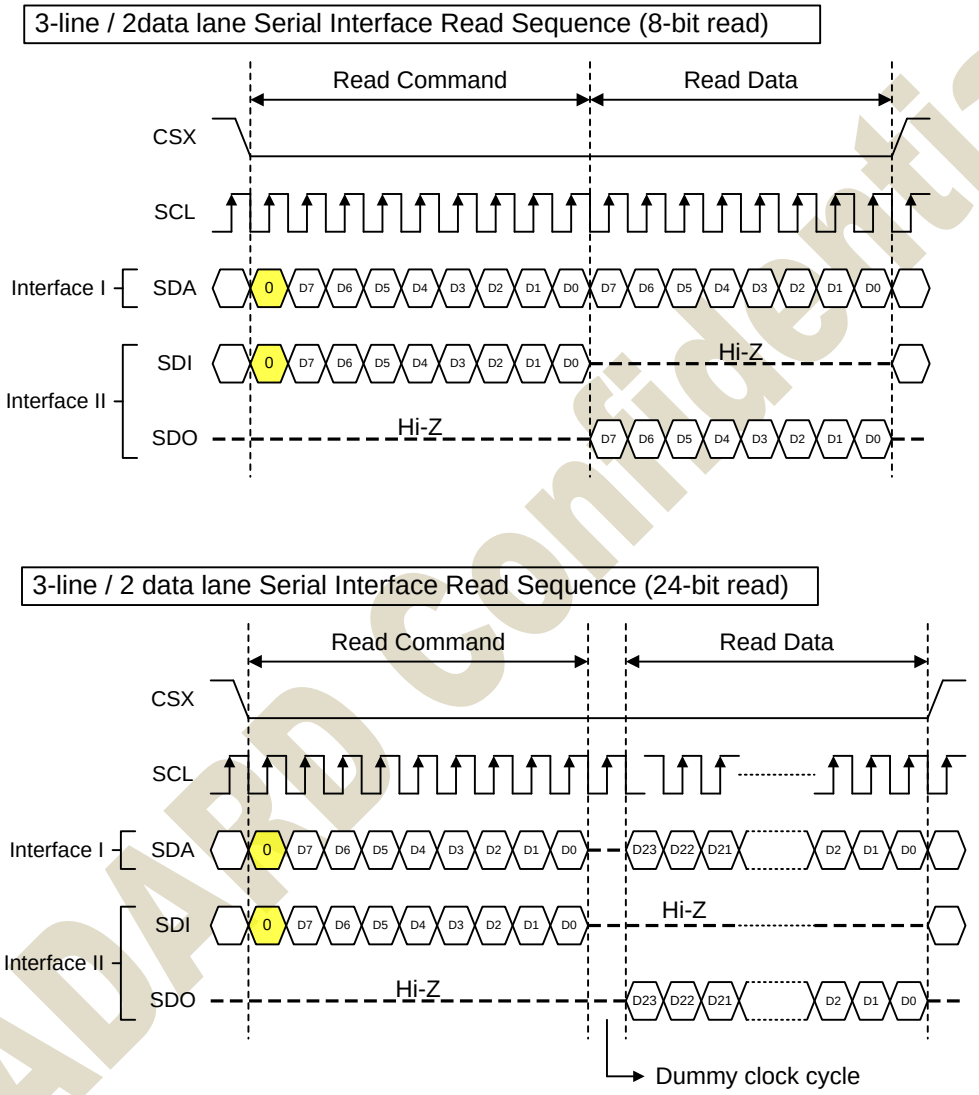


Figure 6.40 Quad serial interface write protocol

6.2.3.2. Read Cycle Sequence

The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. JD9613 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit.



Note: Enter 2 data lane interface the register DSPI_EN=1 and DSPI_CFG[1:0]=01 / 10 / 11

Figure 6.41 3-line / 2data lane serial interface read protocol

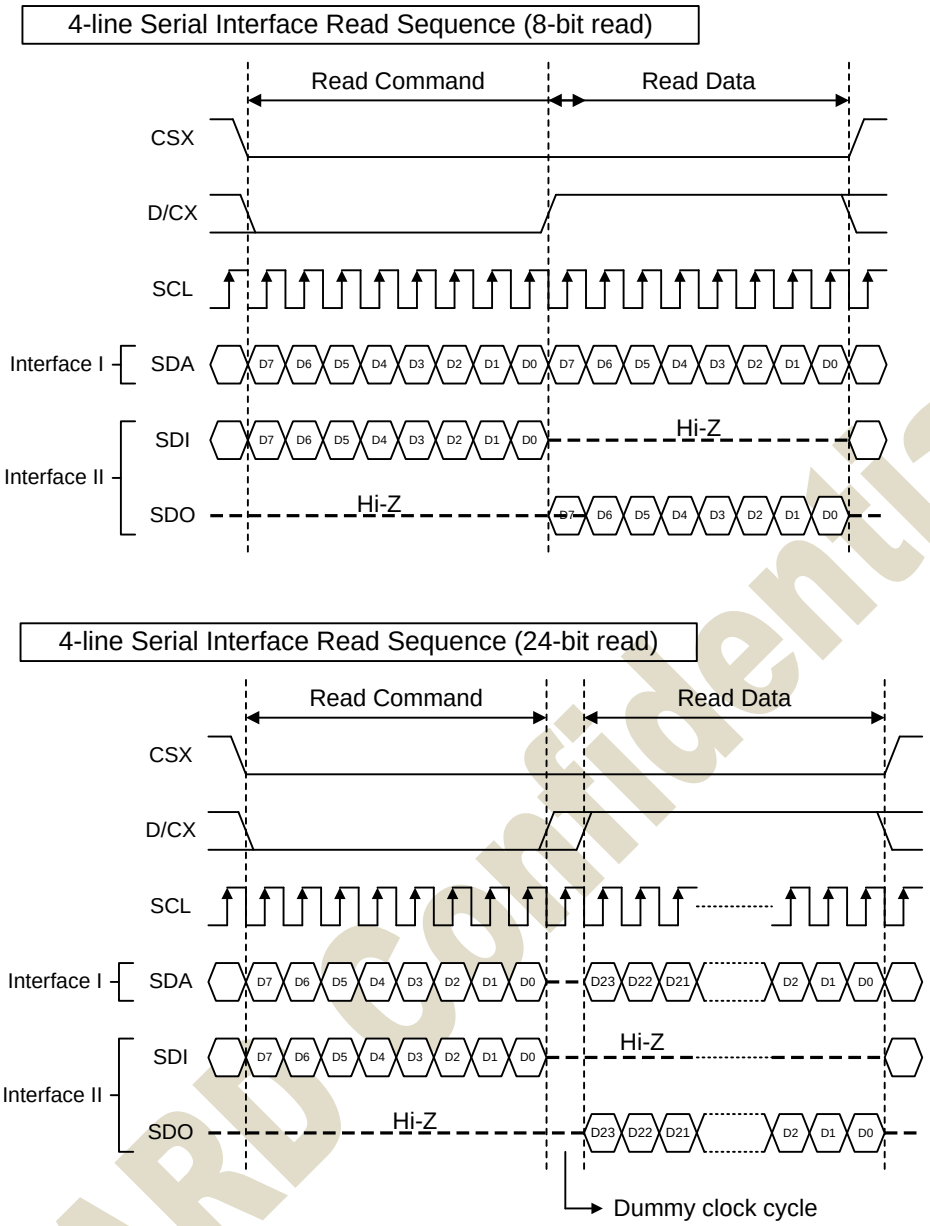


Figure 6.42 4-line serial interface read protocol

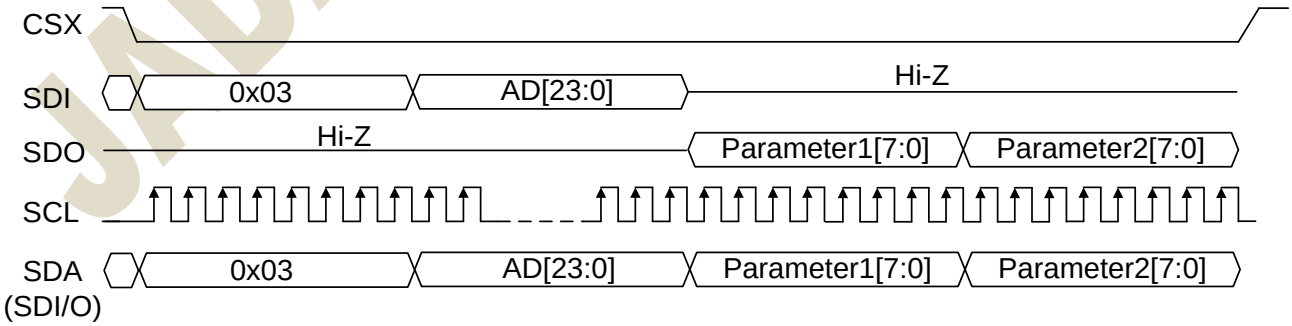
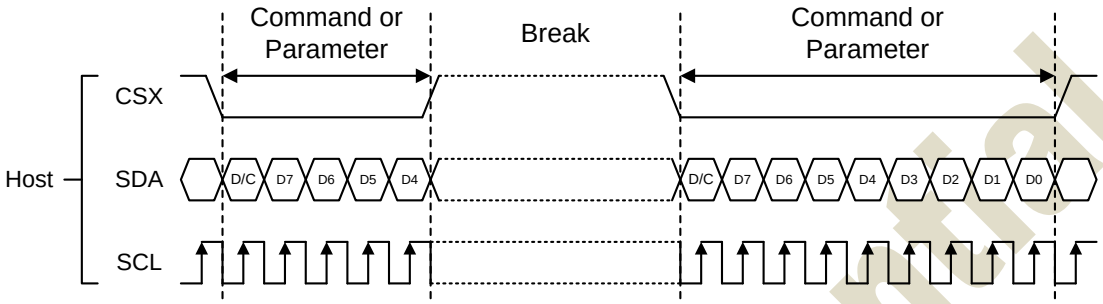


Figure 6.43 Quad serial interface read protocol

6.2.4. Data Transfer Break and Recovery

If there is a break in data transmission while transferring a Command or Parameter or Frame Memory Data before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (CSX) is next activated. See the following example:



If a 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

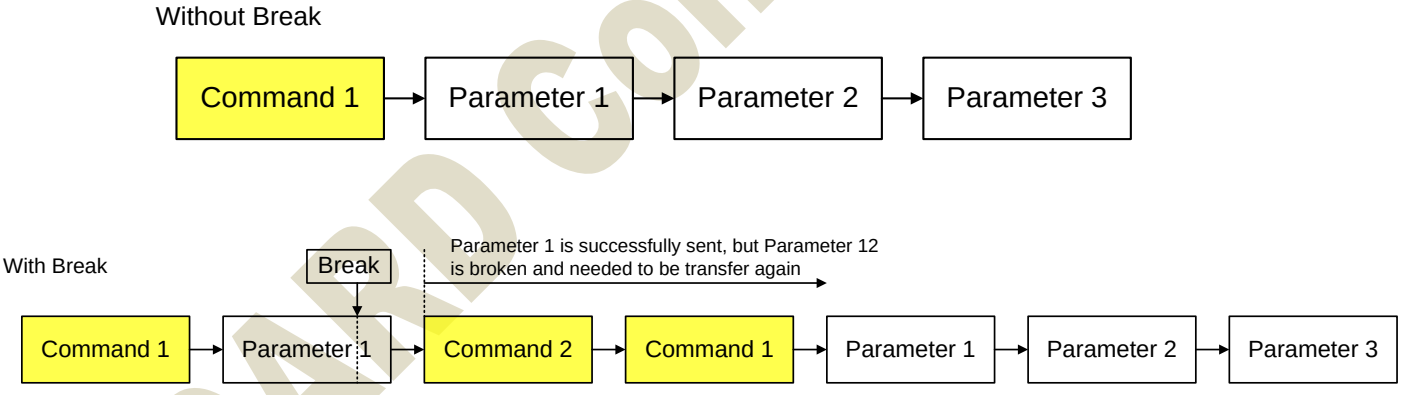


Figure 6.44 Write interrupts recovery, case 1

If a 2 or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

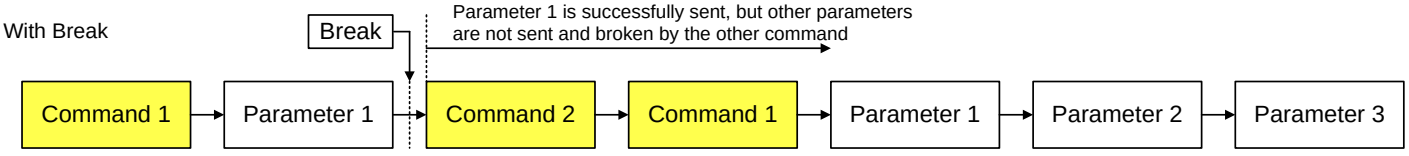


Figure 6.45 Write interrupts recovery, case 2

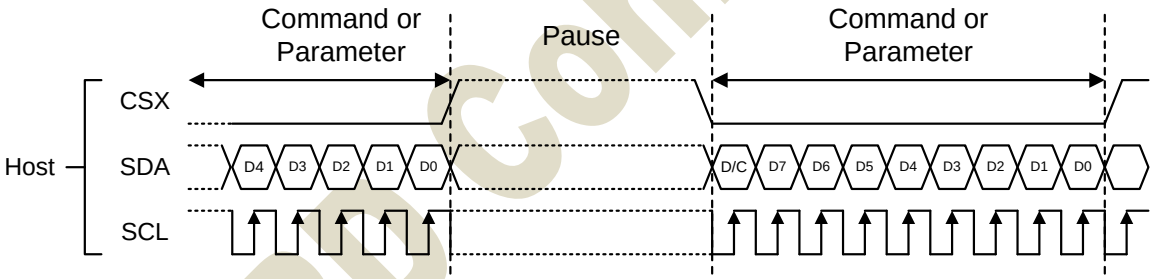
6.2.5. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then JD9613 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

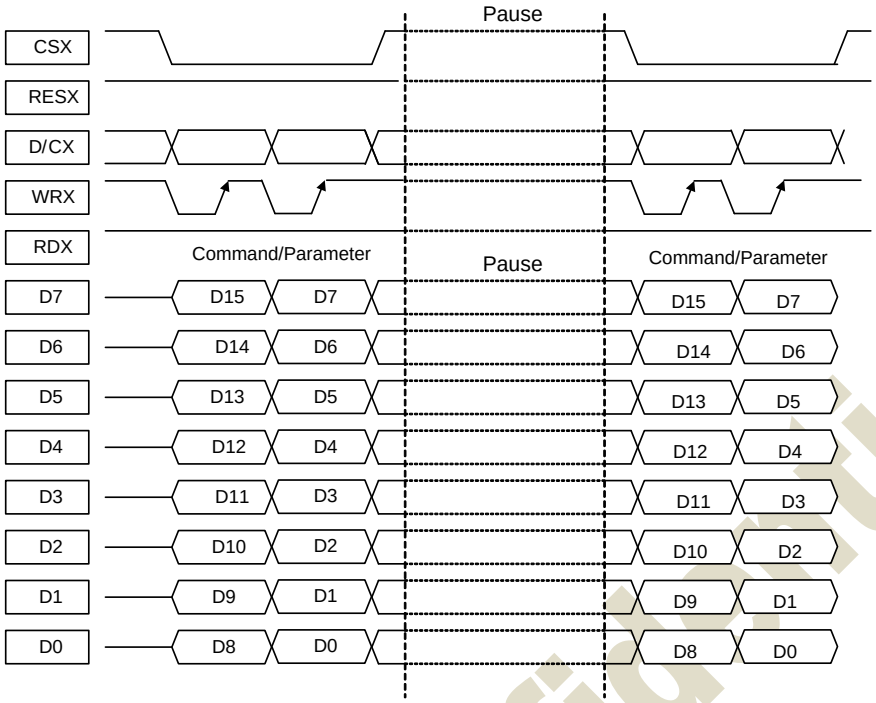
This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

6.2.5.1. Serial Interface Pause



6.2.5.2. Parallel Interface Pause

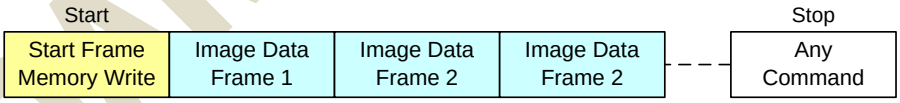


6.2.6. Data Transfer Mode

JD9613 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

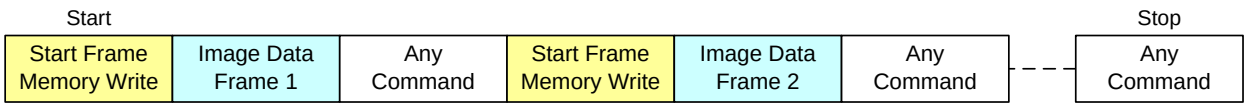
6.2.6.1. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



6.2.6.2. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



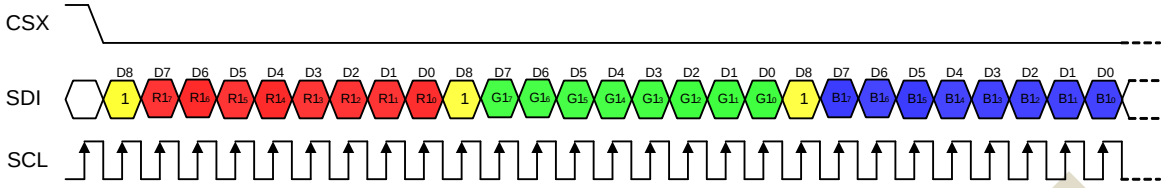
Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

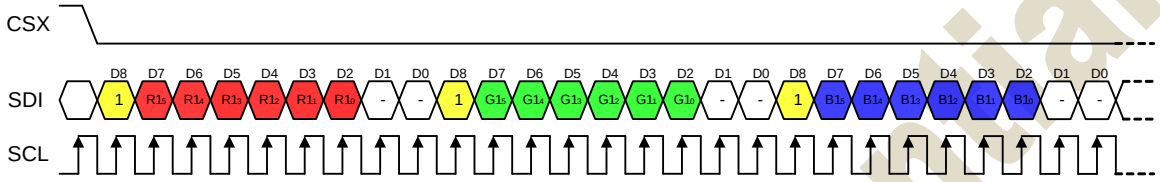
6.2.7. Display Data Format

6.2.7.1. 3-Line Serial Interface

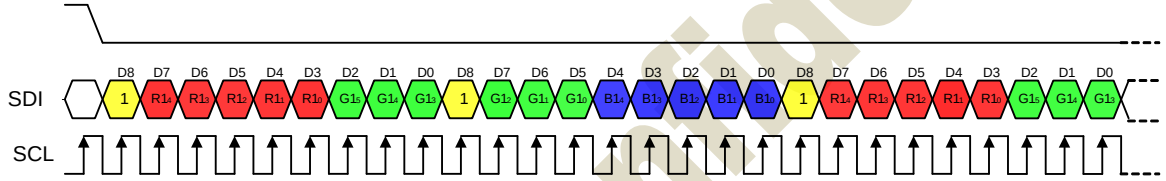
RGB(8-8-8), DSPI_en=0, IFPF=111



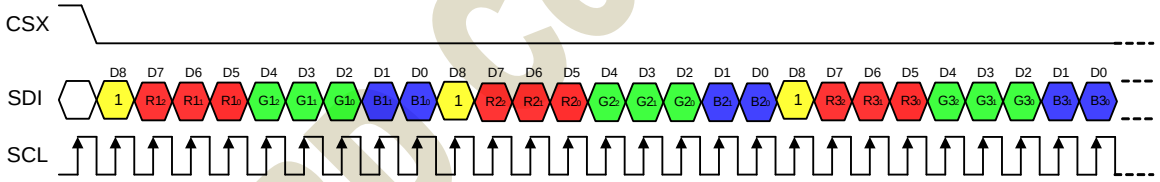
RGB(6-6-6), DSPI_en=0, IFPF=110



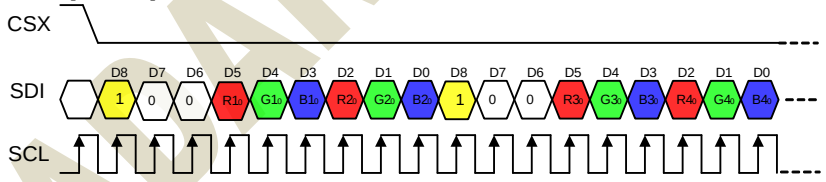
RGB(5-6-5), DSPI_en=0, IFPF=101



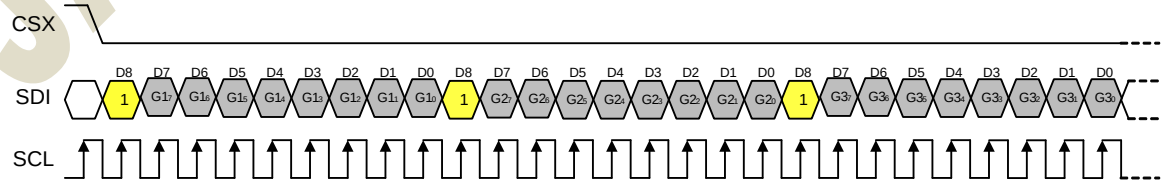
RGB(3-3-2), DSPI_en=0, IFPF=010



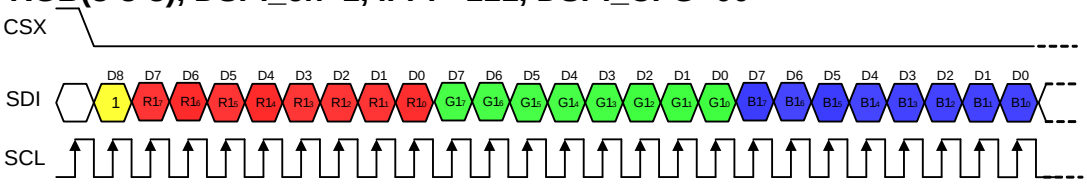
RGB(1-1-1), DSPI_en=0, IFPF=011



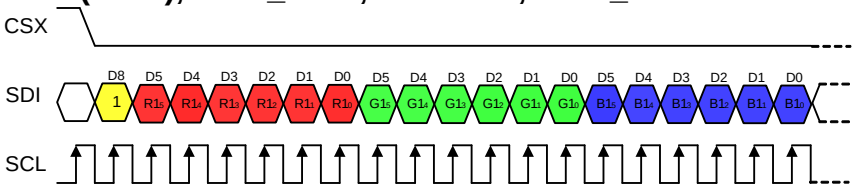
Gray256, DSPI_en=0, IFPF=001



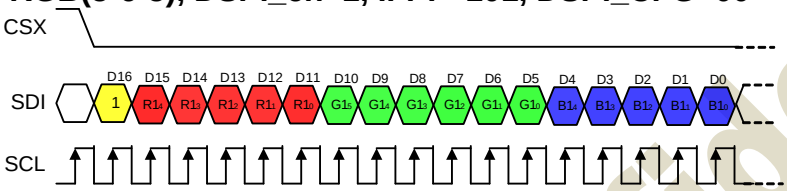
RGB(8-8-8), DSPI_en=1, IFPF=111, DSPI_CFG=00



RGB(6-6-6), DSPI_en=1, IFPF=110, DSPI_CFG=00

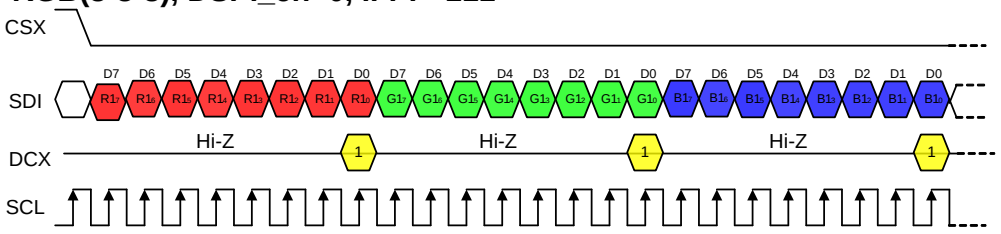


RGB(5-6-5), DSPI_en=1, IFPF=101, DSPI_CFG=00

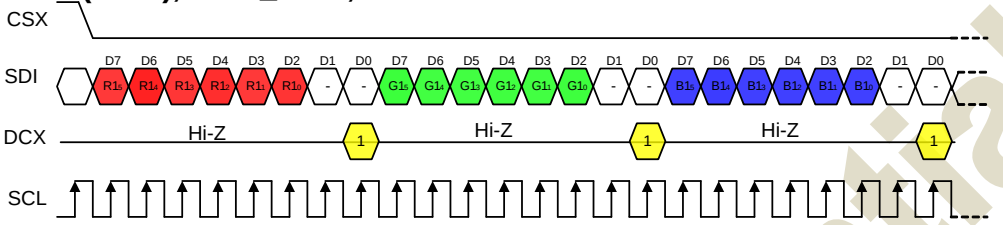


6.2.7.2. 4-Line Serial Interface

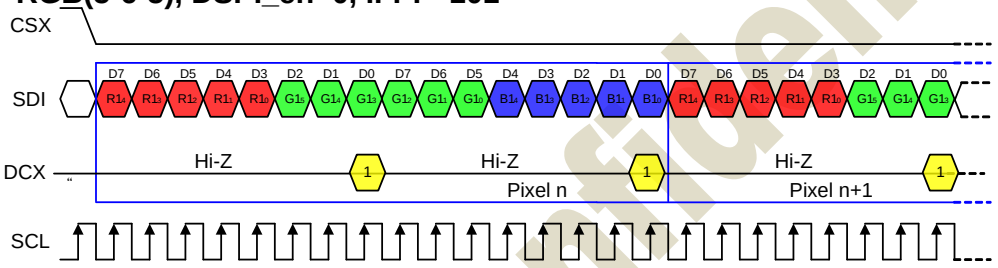
RGB(8-8-8), DSPI_en=0, IFPF=111



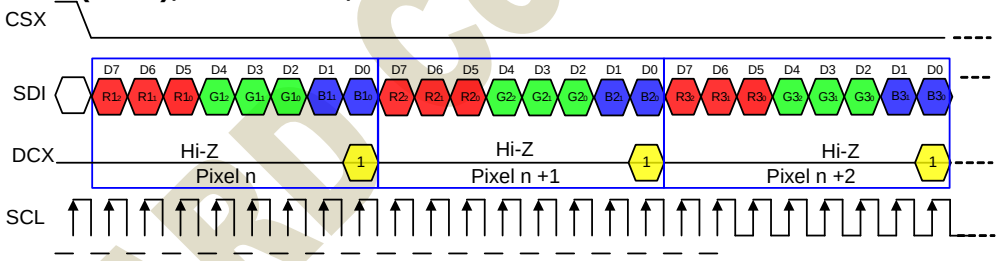
RGB(6-6-6), DSPI_en=0, IFPF=110



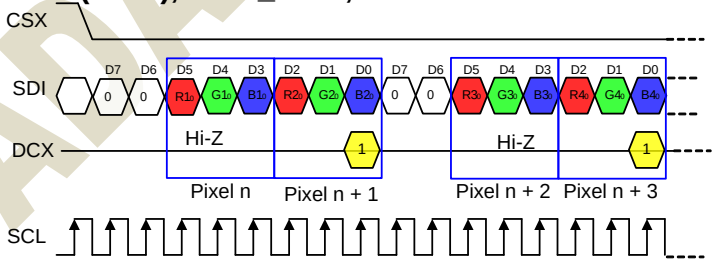
RGB(5-6-5), DSPI_en=0, IFPF=101



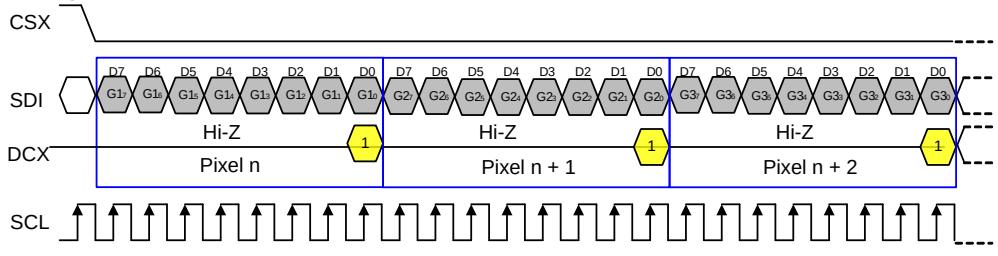
RGB(3-3-2), DSPI_en=0, IFPF=010



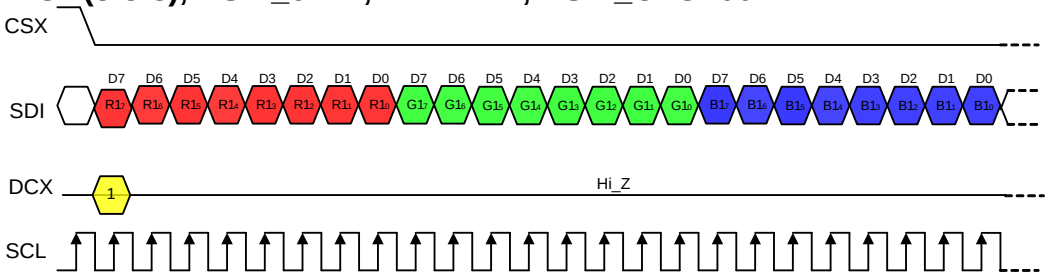
RGB(1-1-1), DSPI_en=0, IFPF=011



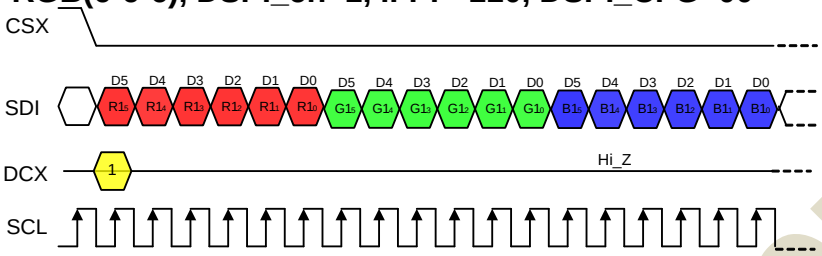
Gray256, DSPI_en=0, IFPF=001



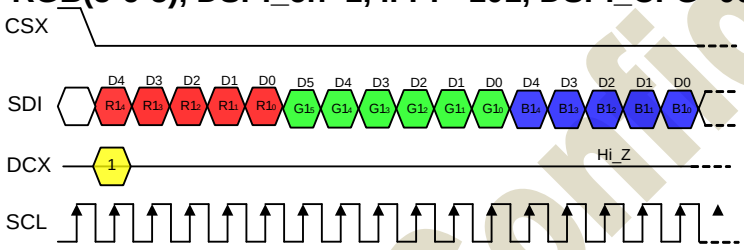
RGB(8-8-8), DSPI_en=1, IFPF=111, DSPI_CFG=00



RGB(6-6-6), DSPI_en=1, IFPF=110, DSPI_CFG=00

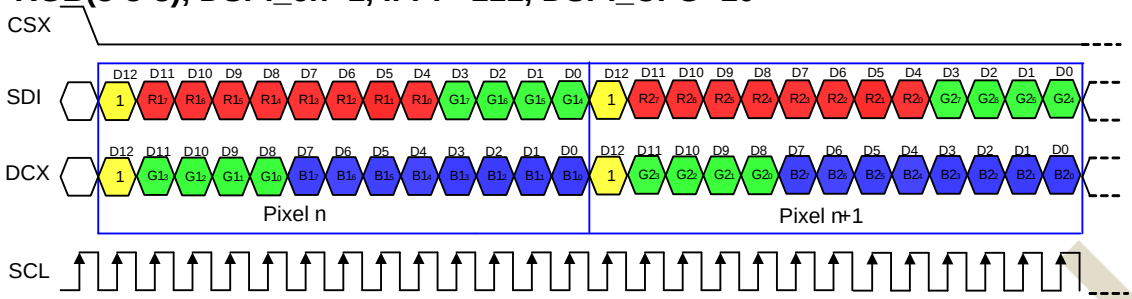


RGB(5-6-5), DSPI_en=1, IFPF=101, DSPI_CFG=00

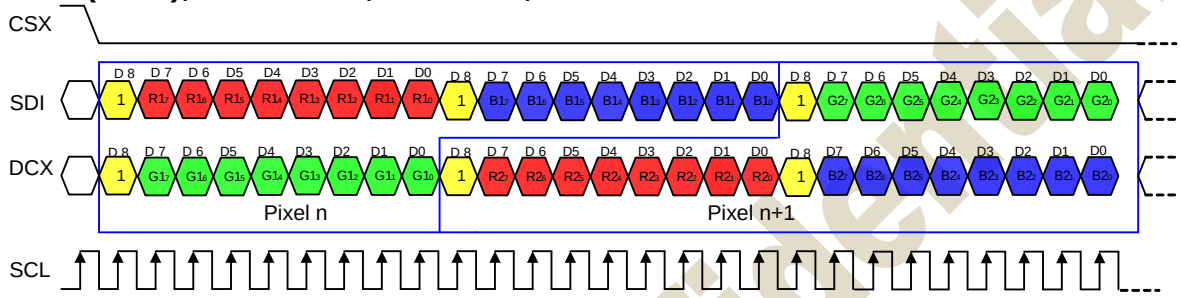


6.2.7.3. 2 data lane Interface

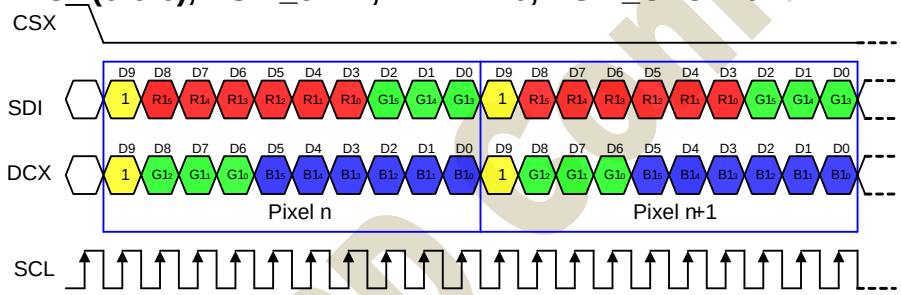
RGB(8-8-8), DSPI_en=1, IFPF=111, DSPI_CFG=10



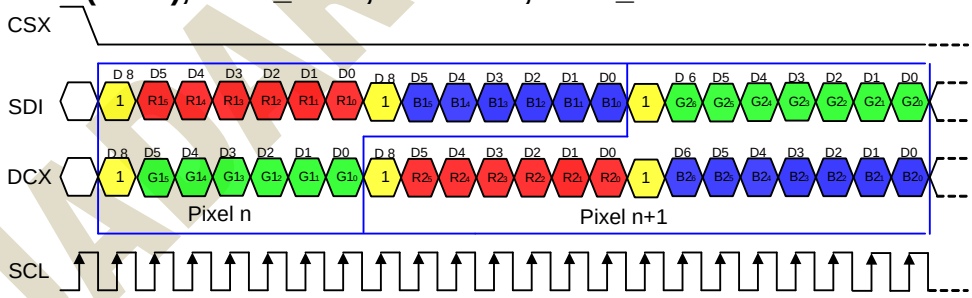
RGB(8-8-8), DSPI_en=1, IFPF=111, DSPI_CFG=11



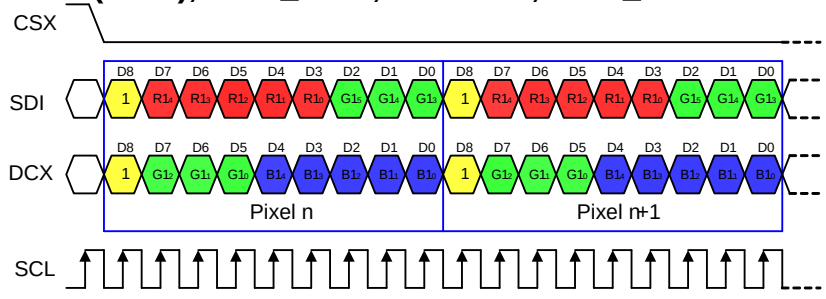
RGB(6-6-6), DSPI_en=1, IFPF=110, DSPI_CFG=10



RGB(6-6-6), DSPI_en=1, IFPF=110, DSPI_CFG=11

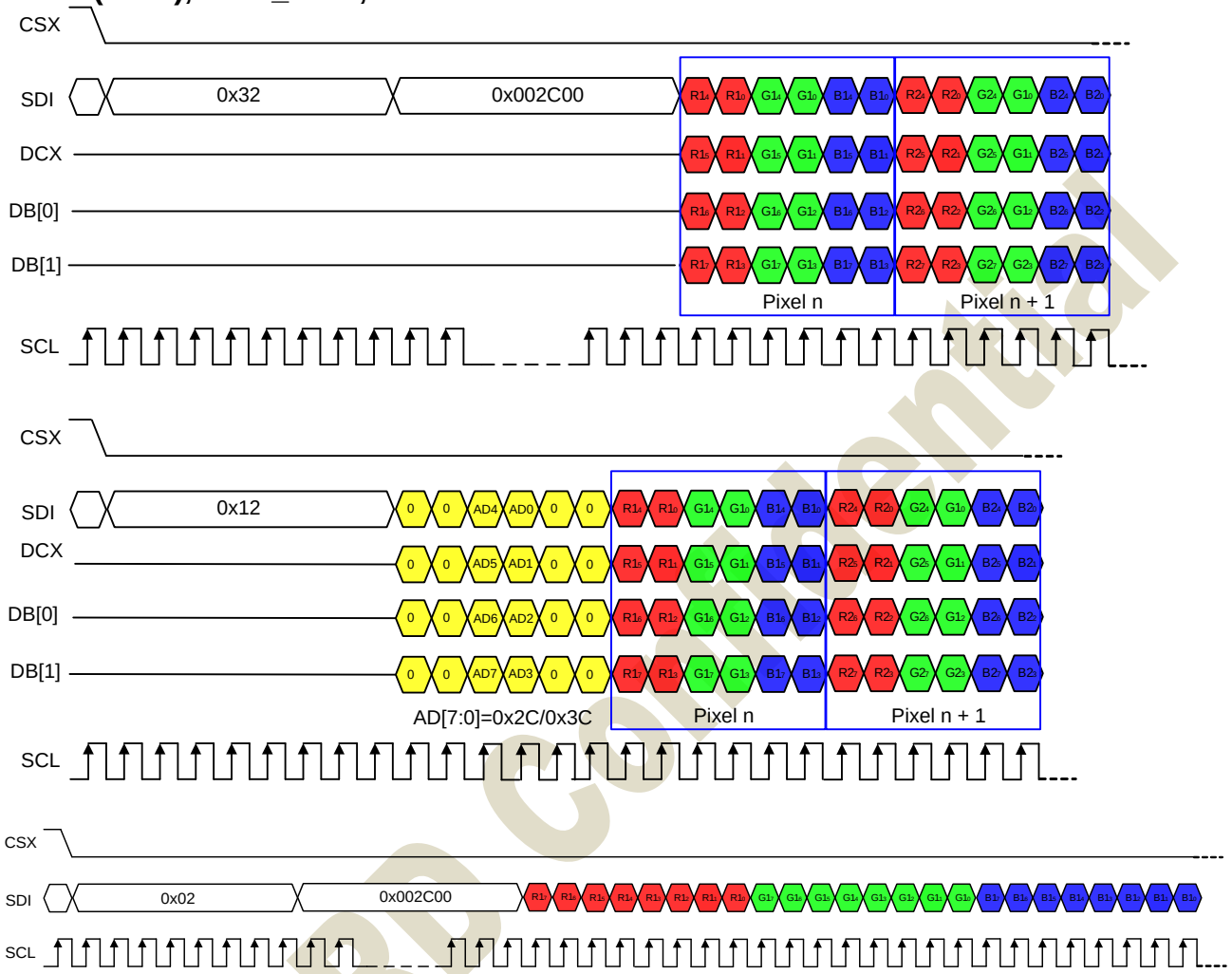


RGB(5-6-5), DSPI_en=1, IFPF=101, DSPI_CFG=10

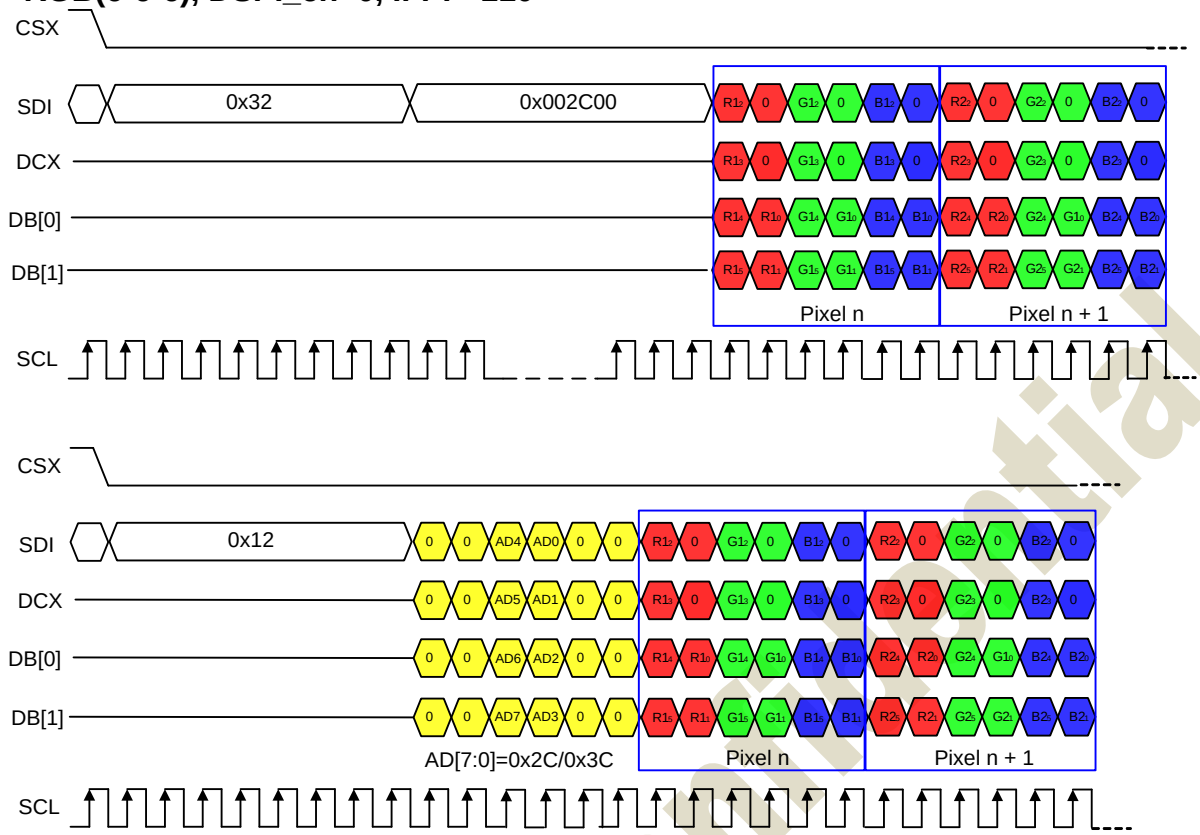


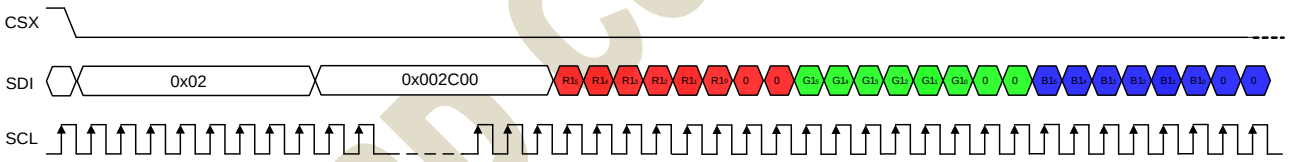
6.2.7.4. Quad Serial Interface

RGB(8-8-8), DSPI_en=0, IFPF=111

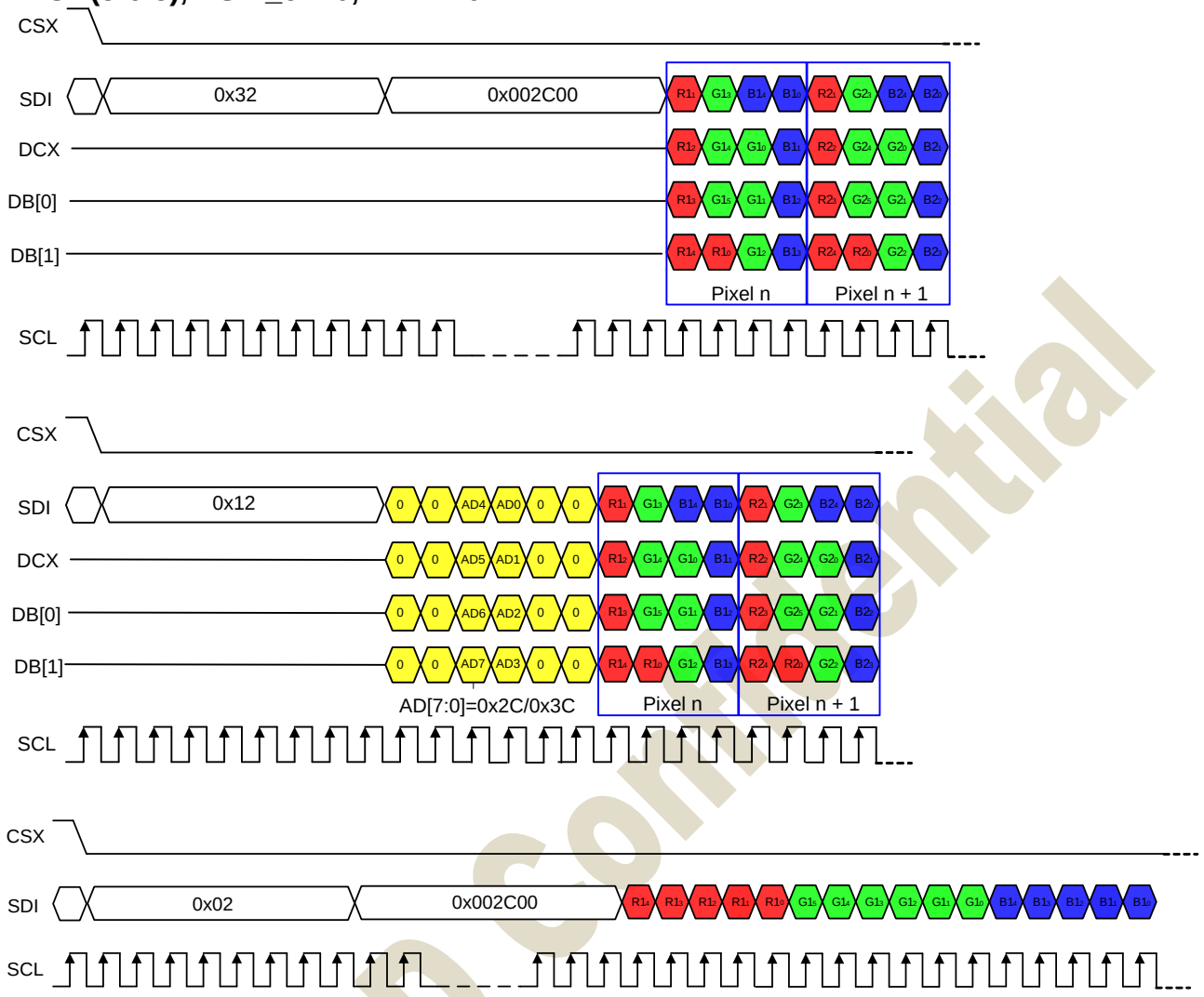


RGB(6-6-6), DSPI_en=0, IFPF=110

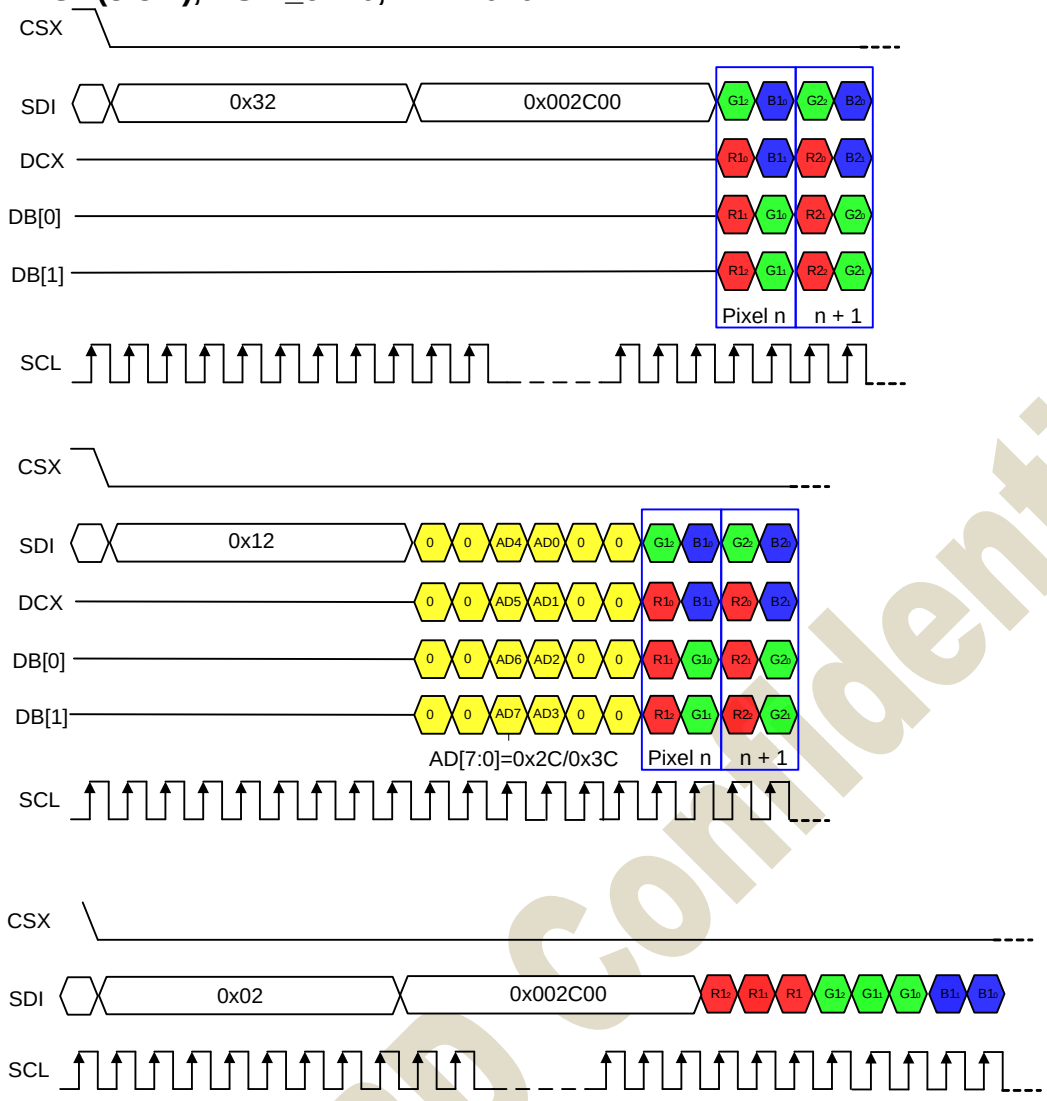




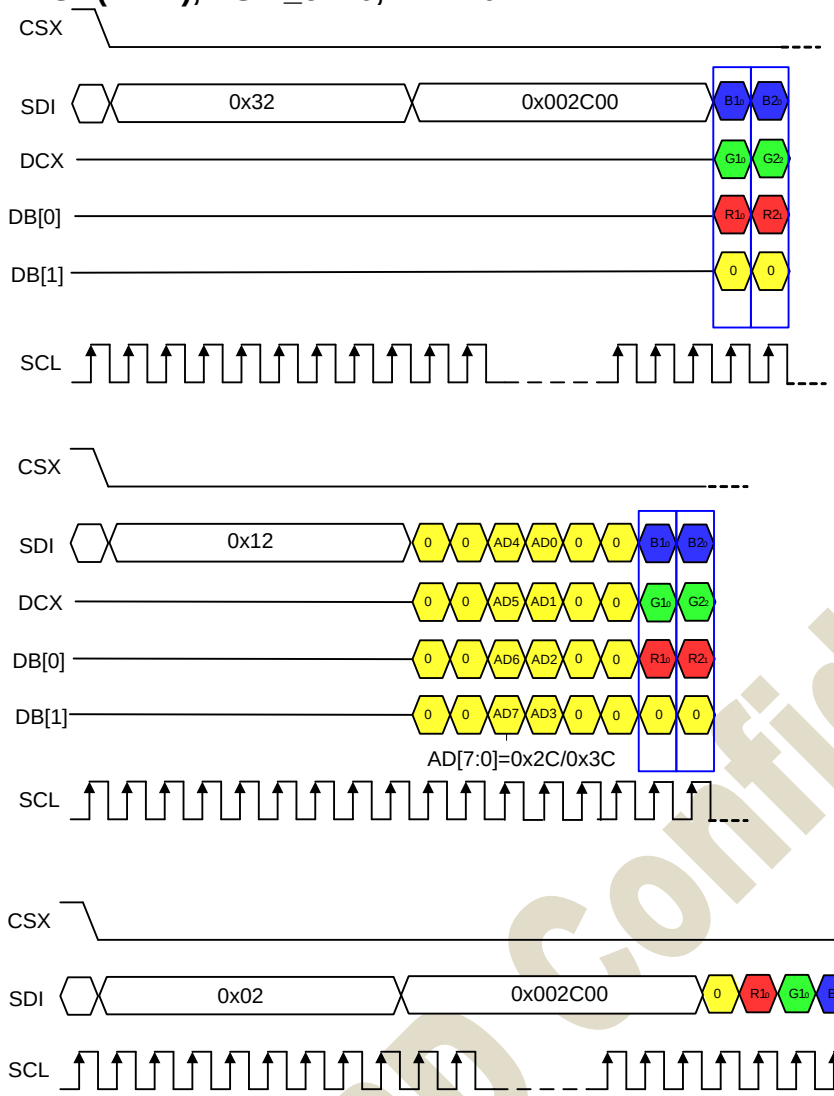
RGB(5-6-5), DSPI_en=0, IFPF=101



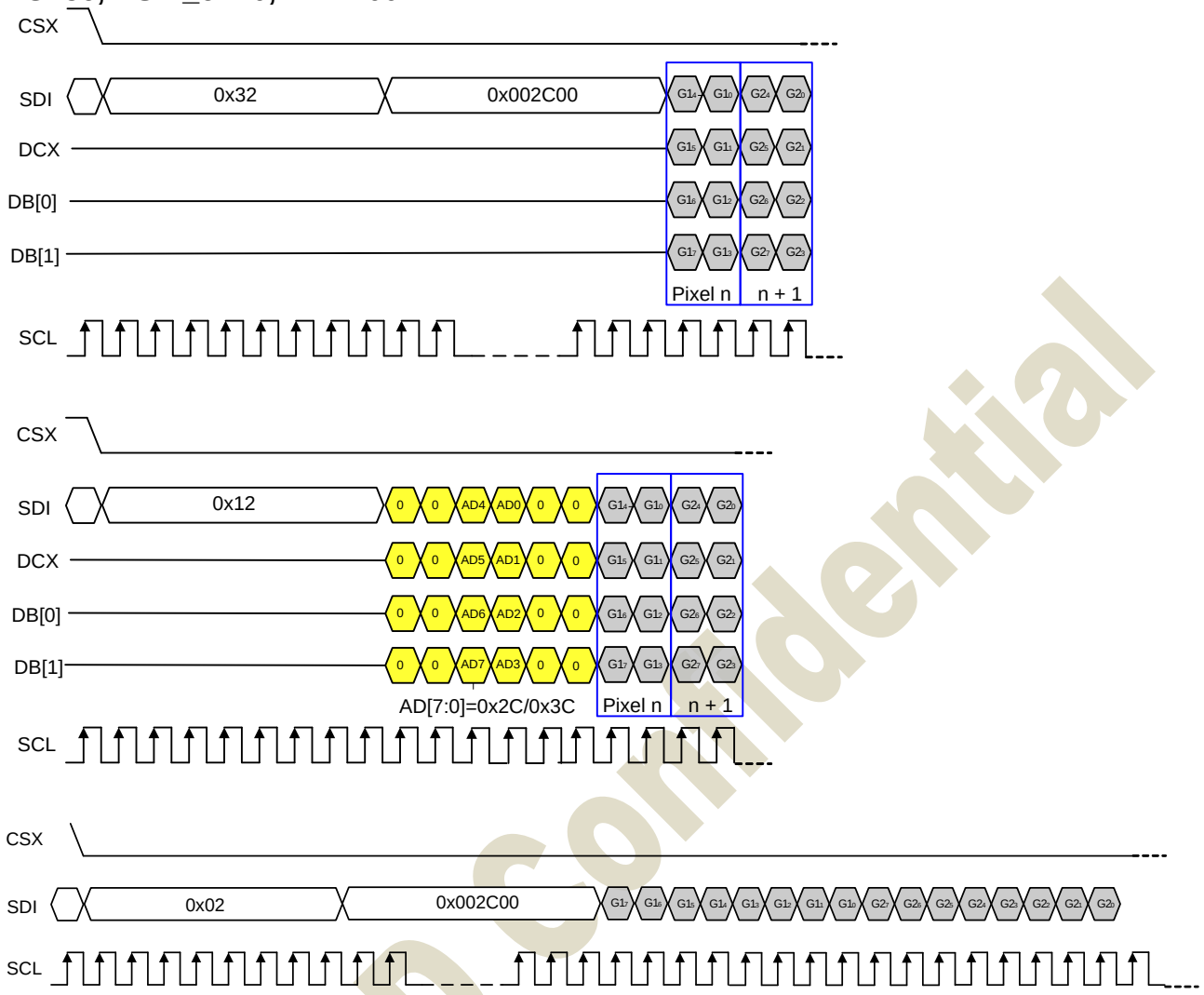
RGB(3-3-2), DSPI_en=0, IFPF=010



RGB(1-1-1), DSPI_en=0, IFPF=011

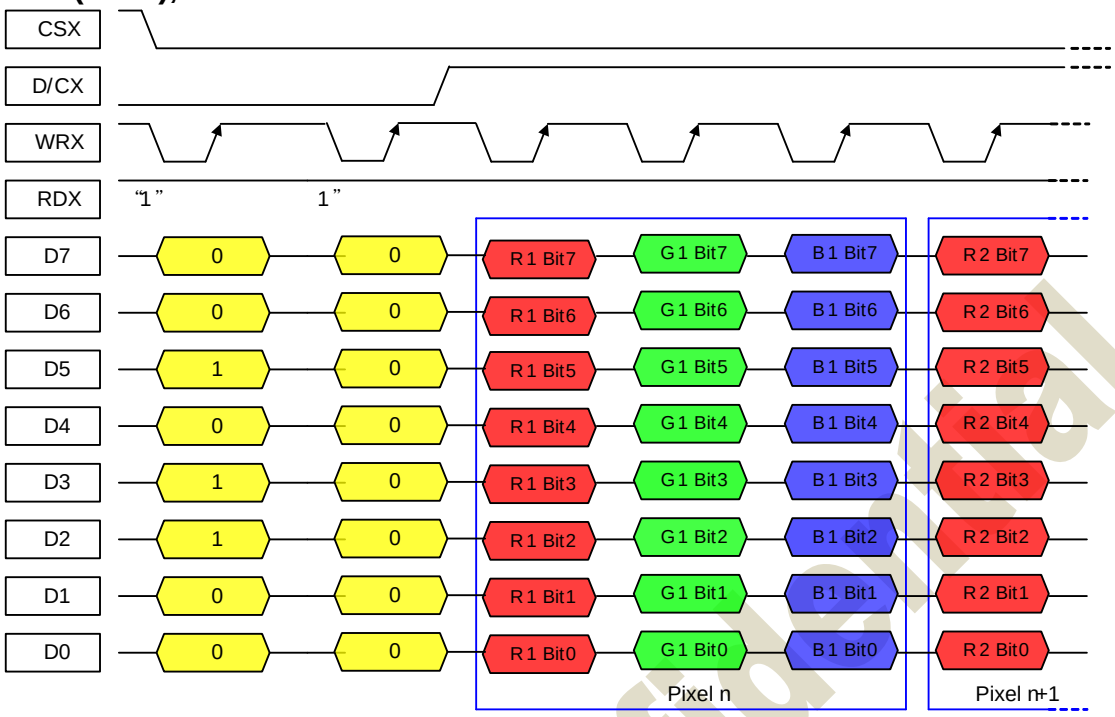


G256, DSPI_en=0, IFPF=001

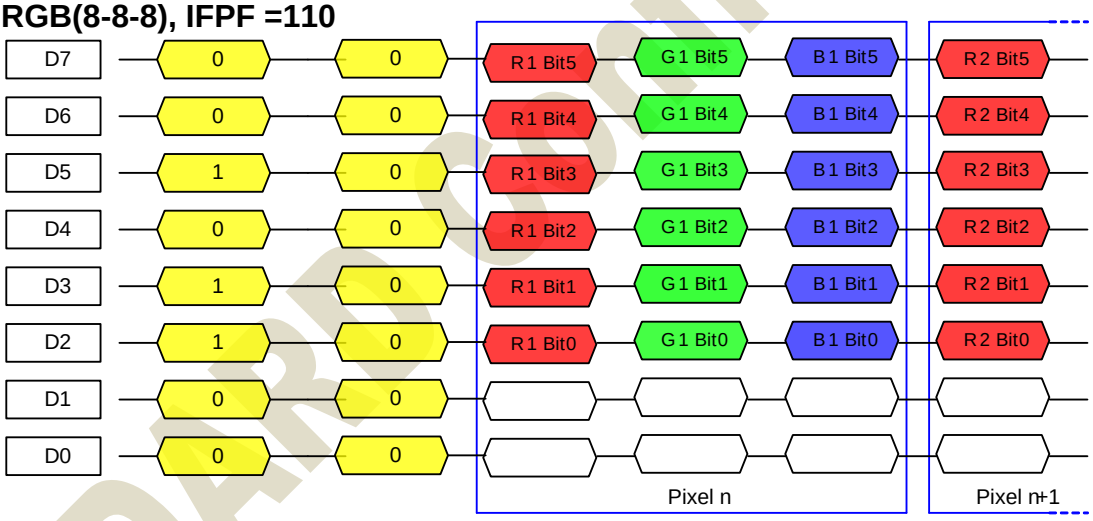


6.2.7.5. 8080-I series 8-bit Parallel Interface

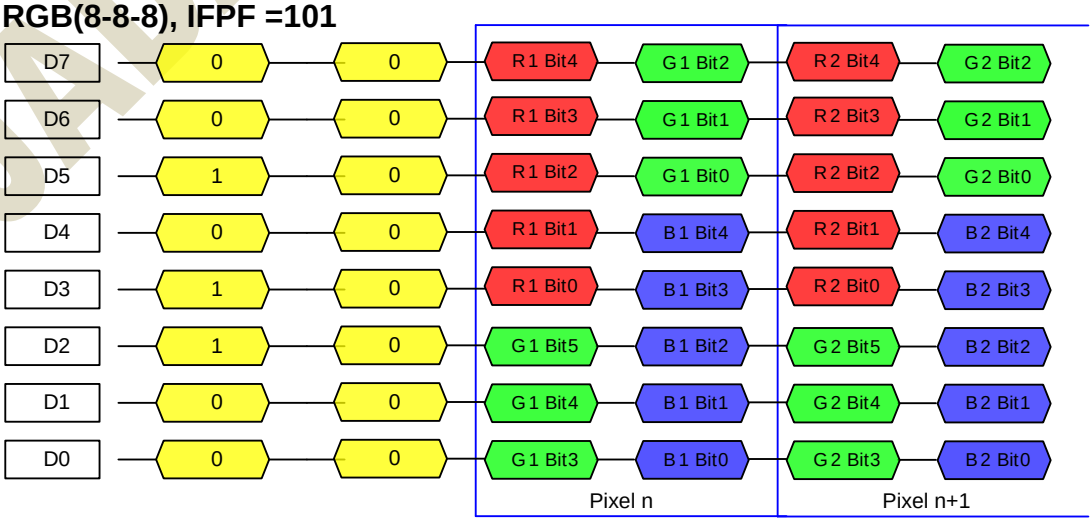
RGB(8-8-8), IFPF =111



RGB(8-8-8), IFPF =110



RGB(8-8-8), IFPF =101

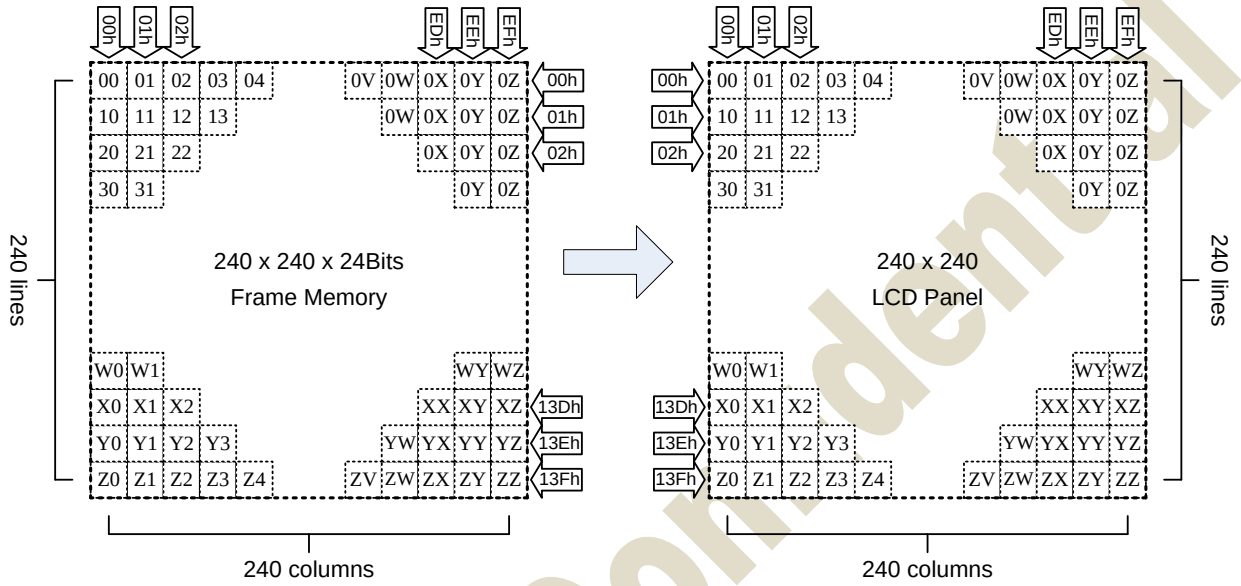


7. Function Description

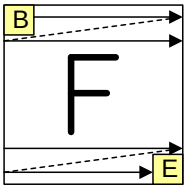
7.1. Memory to Display Address Mapping

7.1.1. Normal Display On or Partial Mode On, Vertical Scroll Off

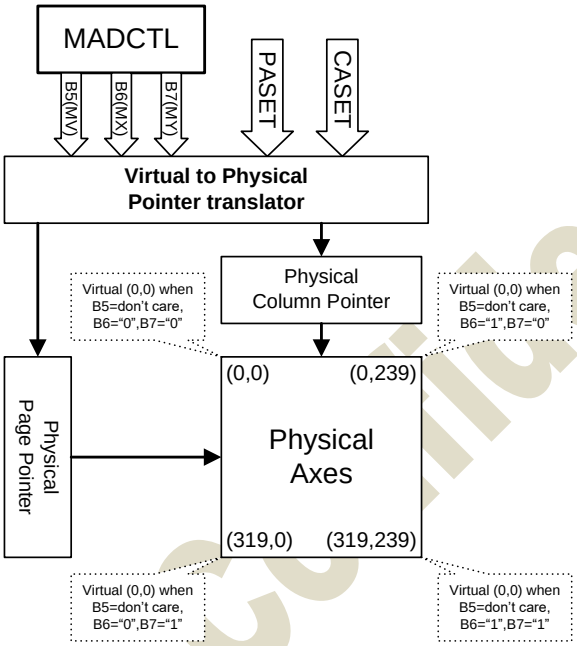
In this mode, contents of the frame memory within an area where column pointer is 00h to EFh and page pointer is 00h to EFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0).



7.2. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command(36h), Bits B5, B6, B7(MV, MX, MY) as described below.

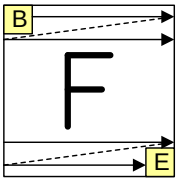
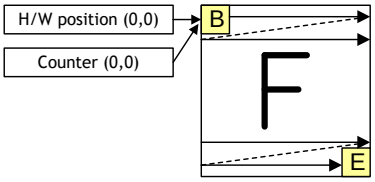
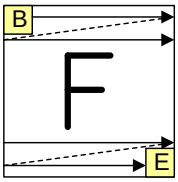
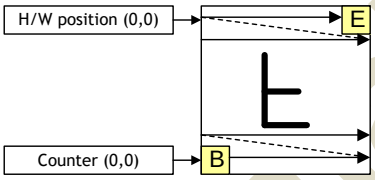
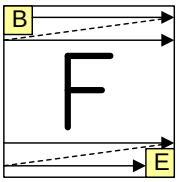
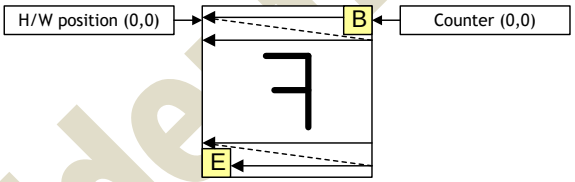
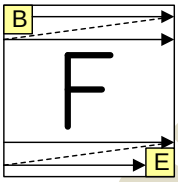
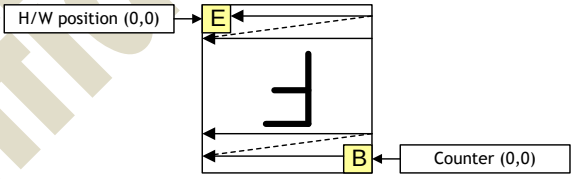
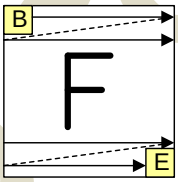
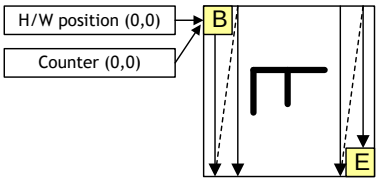
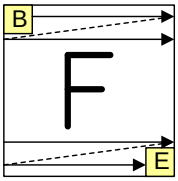
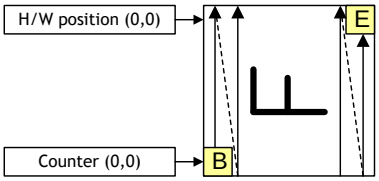
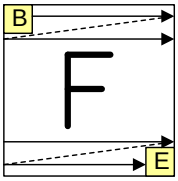
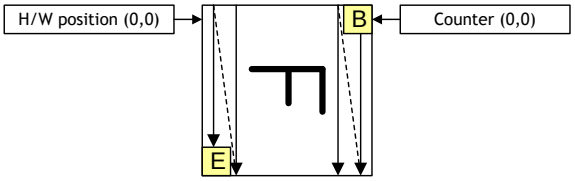
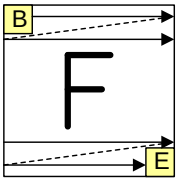
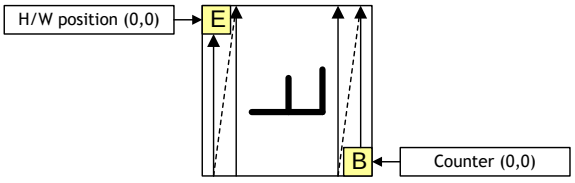


B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to “Start Column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End column.”	Return to “Start Column”	Increment by 1
The Column counter value is larger than “End column” and the Page counter value is larger than “End page”.	Return to “Start Column”	Return to “Start Page”

The resultant image for each setting is illustrated below:

Display Data Direction	MADCTL			Image in the Host	Image in Frame Memory
	MV	MX	MY		
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-Invert	1	0	1		
X-Y exchange X-Invert	1	1	0		
X-Y exchange X-Invert Y-Invert	1	1	1		

7.3. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.3.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:

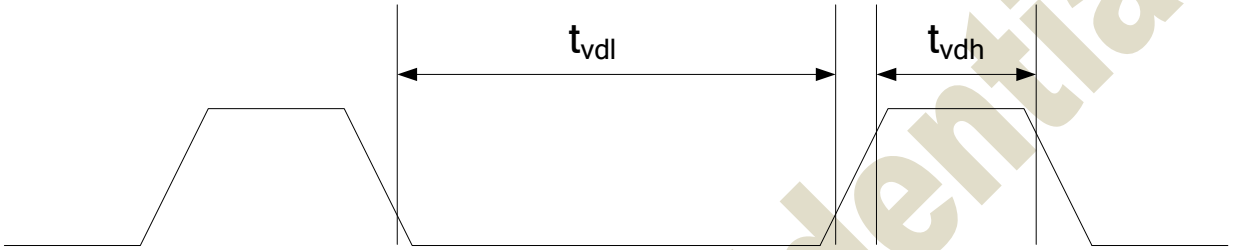


Figure 7.1 Tearing Effect Line mode 1

tvdh= The AMOLED display is not updated from the Frame Memory
tvdl= The AMOLED display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-sync and H-sync Information, there is one V-sync and N H-sync pulses per field.
N: If the resolution is 240 RGB X 240, the N=240.

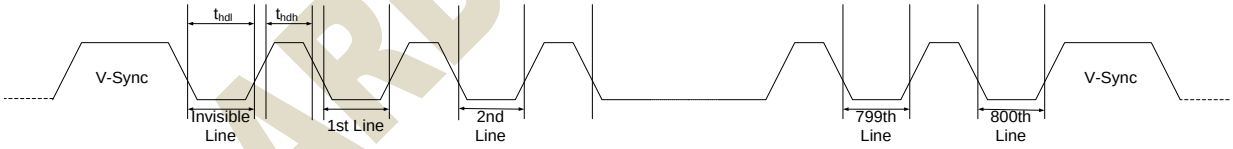


Figure 7.2 Tearing Effect Line mode 2

thdh= The AMOLED display is not updated from the Frame Memory
thdl= The AMOLED display is updated from the Frame Memory (except Invisible Line – see above)

Mode 3, turn on the Tearing Effect Output signal when vertical scanning reaches line N

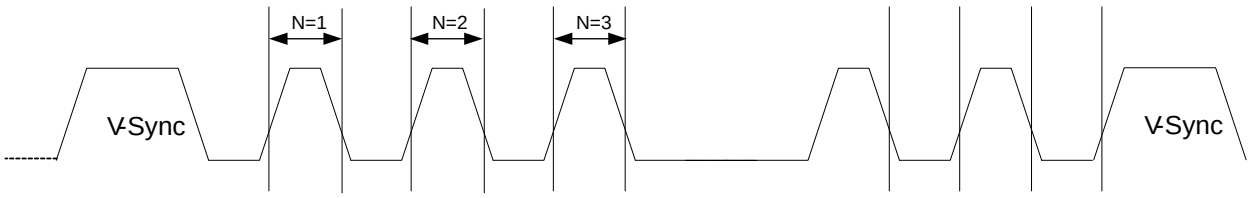


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Figure 7.3 Tearing Effect Line mode 2

N= The N-th scanning line which set by register N[15:0] of command STESL(44h)

7.3.2. Tearing effect line timing

The Tearing Effect signal is described below.

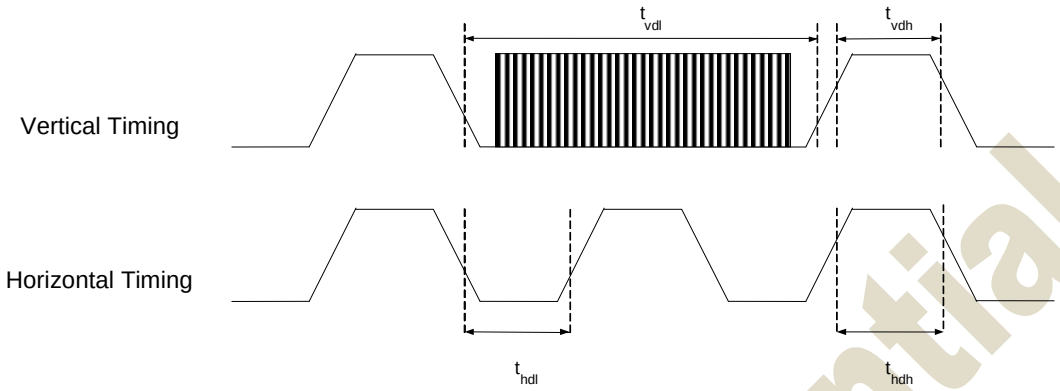


Figure 7.4 Tearing Effect Line timing

Idle Mode Off/On (Frame Rate = 60 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	TBD	-	ms
tvdh	Vertical Timing High Duration	1000	-	us
thdl	Horizontal Timing Low Duration	TBD	-	us
thdh	Horizontal Timing High Duration	TBD	500	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	Ns

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

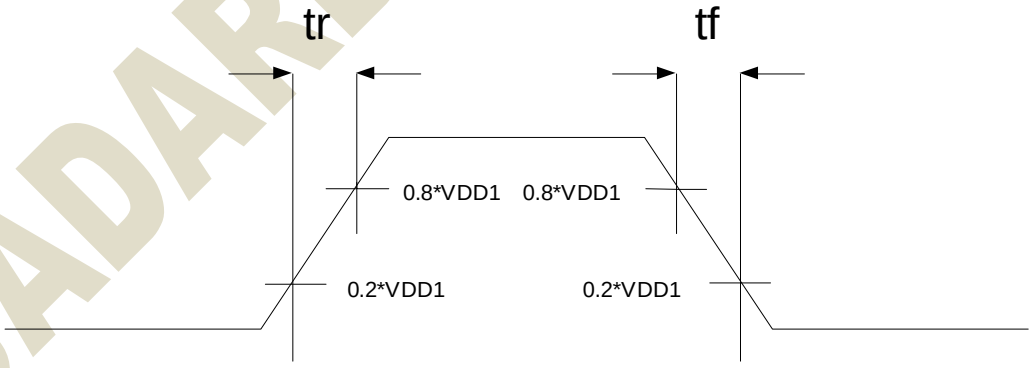
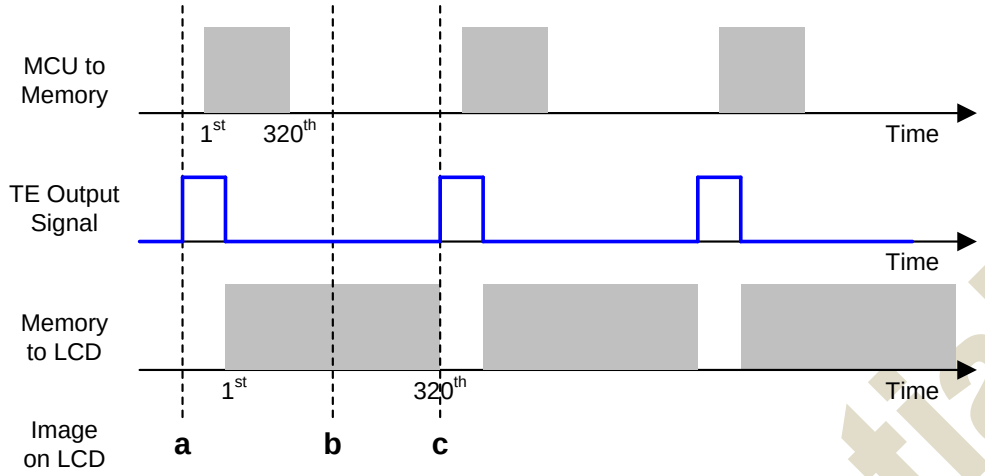


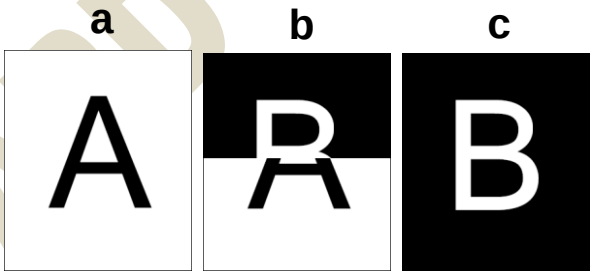
Figure 7.5 Tearing Effect Line definition of tf, tr

7.3.3. Example1: MCU Write is faster than panel read

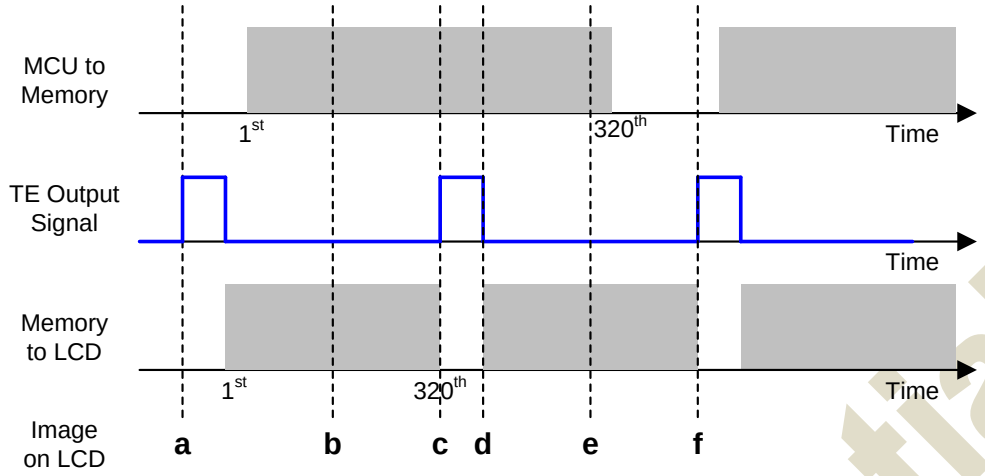


Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

Data to be Send 

Image on AMOLED 

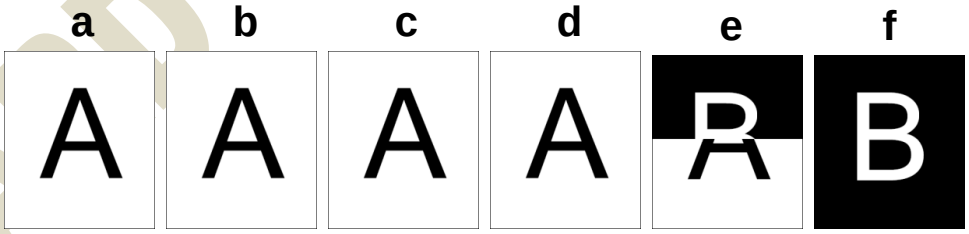
7.3.4. Example2: MCU Write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

Data to be Send

Image on AMOLED



7.4. Oscillator

The JD9613 has an internal R-C oscillator. The oscillator frequency is 16MHz and tolerance is 5% (at 25° C). The oscillation frequency can be adjusted according to internal register setting.

7.5. Adjustable Digital Gamma

The JD9613 includes gamma adjustment function for the 262k colors display . Gamma adjustment operation is implemented by 27 digital gamma adjustment control registers and 12bits digital gamma register to meet the characteristic of AMOLED panel.

7.6. Power on/off sequence

7.6.1. General

IOVCC must be setup ready before analog power setup.
IOVCC must be power down after analog power down.

During power off, if the display module is in the SLPOUT mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the SLPIN mode, VCI and IOVCC can be powered down minimum 0msec after RESX has been released.

There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display panel between end of Power On Sequence and before receiving SLPOUT command. Also, between receiving SLPOUT command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.6.1, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

There is not a limit for Rise/Fall time on VCI, VCIP and IOVCC.

7.6.2. Power on/off sequence

Power on sequence:

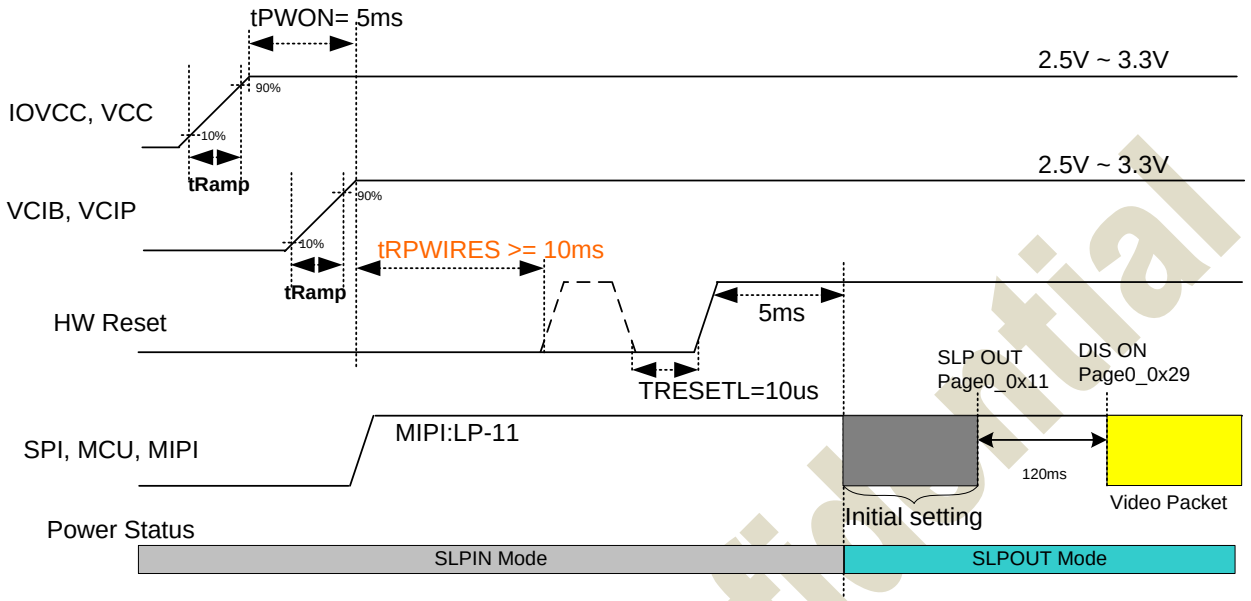


Figure 7.6 Power on sequence

	Min	Typ	Max
Power up tRamp for IOVCC / VCI	0.2ms		20ms

Power off sequence 1:

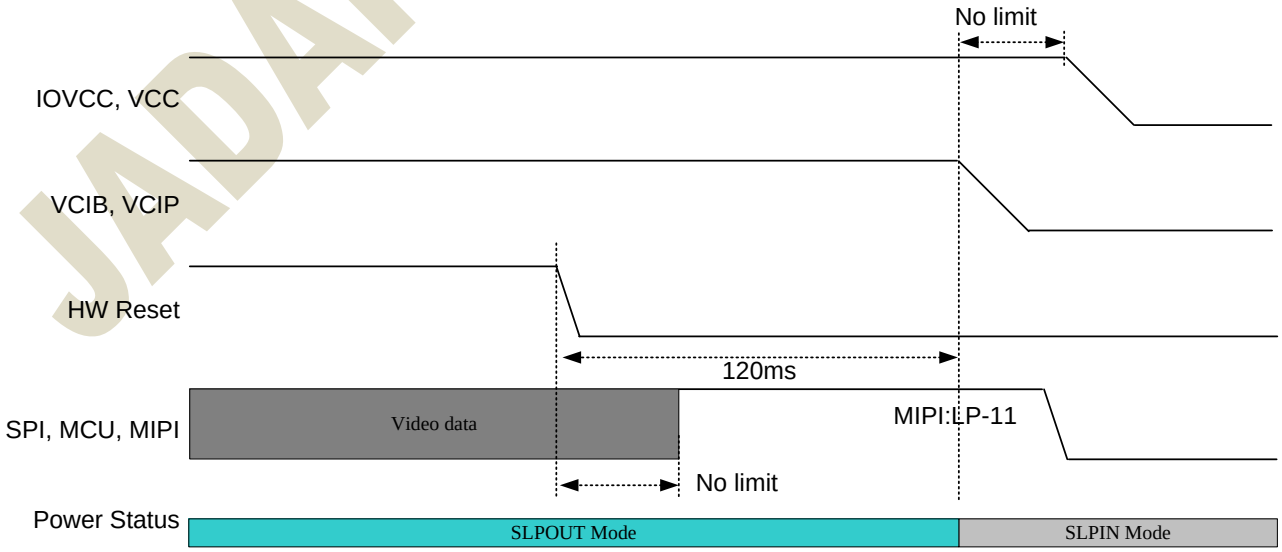


Figure 7.7 Power off sequence 1

Power off sequence 2:

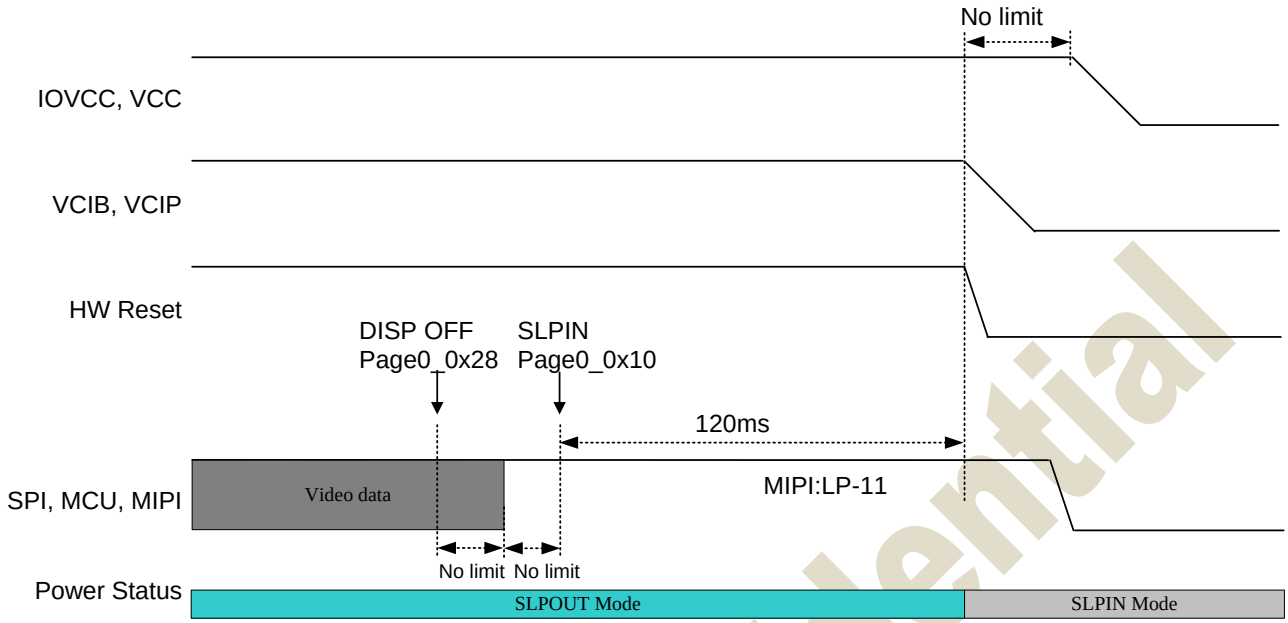
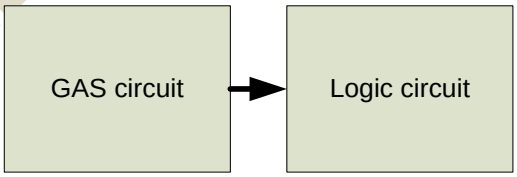


Figure 7.8 Power off sequence 2

7.7. Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

- There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.
- There cannot be any abnormal visible effects (= display must be blank) with in 1 second on the display and remains blank until “Power On Sequence” powers it up



8. Command

8.1. Command List

8.1.1. Standard command

Address	Operation code	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Function
00	NOP	W	0	0	0	0	0	0	0	0	No Operation
01	SWRESET	W	0	0	0	0	0	0	0	1	Software Reset
04	RDDIDIF	W	0	0	0	0	0	1	0	0	Read Display Identification Information
		R	ID1[7:0]								
		R	ID2[7:0]								
		R	ID3[7:0]								
05	RDNUMPE	W	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error
		R	P[7:0]								
06	RDRED	W	0	0	0	0	0	1	1	0	Read Red Color
		R	R[7:0]								
07	RDGREEN	W	0	0	0	0	0	1	1	1	Read Green Color
		R	G[7:0]								
08	RDBLUE	W	0	0	0	0	1	0	0	0	Read Blue Color
		R	B[7:0]								
09	RDDST	W	0	0	0	0	1	0	0	1	Read Display Status
		R	D[31:24]								
		R	D[23:16]								
		R	D[15:8]								
		R	D[7:0]								
0A	RDDPM	W	0	0	0	0	1	0	1	0	Read display power mode
		R	D7	D6	D5	D4	D3	D2	0	0	
0B	RDDMADCTL	W	0	0	0	0	1	0	1	1	Read display MADCTL
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0C	RDDCOLMOD	W	0	0	0	0	1	1	0	0	Read display pixel format
		R	0	D6	D5	D4	0	D2	D1	D0	
0D	RDDIM	W	0	0	0	0	1	1	0	1	Read display image mode
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0E	RDDSM	W	0	0	0	0	1	1	1	0	Read display signal mode
		R	D7	D6	D5	D4	D3	D2	D1	D0	
0F	RDDSDR	W	0	0	0	0	1	1	1	1	Read display self-diagnostic result
		R	D7	D6	D5	D4	0	0	0	D0	

10	SLPIN	W	0	0	0	1	0	0	0	0	Sleep In
11	SLPOUT	W	0	0	0	1	0	0	0	1	Sleep Out
12	PTLON	W	0	0	0	1	0	0	1	0	Partial Mode On
13	NORON	W	0	0	0	1	0	0	1	1	Normal display mode on
22	ALLPOFF	W	0	0	1	0	0	0	1	0	All Pixel Off
23	ALLPON	W	0	0	1	0	0	0	1	1	All Pixel On
26	GAMSET	W	0	0	1	0	0	1	1	0	Gamma set-
		W	CG[7:0]								
28	DISPOFF	W	0	0	1	0	1	0	0	0	Display off
29	DISPON	W	0	0	1	0	1	0	0	1	Display on
2A	CASET	W	0	0	1	0	1	0	1	0	Column Address Set
		W	SC[15:8]								Column address start
		W	SC[7:0]								
		W	EC[15:8]								Column address end
		W	EC[7:0]								
2B	PASET	W	0	0	1	0	1	0	1	1	Page address set
		W	SP[15:8]								Page address start
		W	SP[7:0]								
		W	EP[15:8]								Page address end
		W	EP[7:0]								
2C	RAMWR	W	0	0	1	0	1	1	0	0	Memory Write
		W	D1[7:0]								Write data
		W	……								
		W	Dn[7:0]								
30	PLTAR	W	0	0	1	1	0	0	0	0	Partial Area
		W	SR[15:8]								Start row
		W	SR[7:0]								
		W	ER[15:8]								End row
		W	ER[7:0]								
31	VPLTAR	W	0	0	1	1	0	0	0	0	Vertical Partial Area
		W	PSC[15:8]								Start column
		W	PSC[7:0]								
		W	PEC[15:8]								End column
		W	PEC[7:0]								
34	TEOFF	W	0	0	1	1	0	1	0	0	Tearing Effect Line OFF
35	TEON	W	0	0	1	1	0	1	0	1	Tearing Effect Line ON
		W	X	X	X	X	X	X	X	M	

36	MADCTL	W	0	0	1	1	0	1	1	0	Memory Access Control
		W	MY	MX	X	X	BGR	-	SS	GS	
38	IDMOFF	W	0	0	1	1	1	0	0	0	Idle mode off
39	IDMON	W	0	0	1	1	1	0	0	1	Idle mode on
3A	COLMOD	W	0	0	1	1	1	0	1	0	Interface Pixel Format,
		W	X	D6	D5	D4	X	X	X	X	
3C	RAMWRCON	W	0	0	1	1	1	1	0	0	Memory Write Continue
		W	D1[7:0]								Write data
		W	……								
		W	Dn[7:0]								
44	TESL	W	0	1	0	0	0	1	0	0	Set Tear Effect Scan Lines
		W	TELINE[15:8]								
		W	TELINE[7:0]								
45	GETSCAN	W	0	1	0	0	0	1	0	1	Return the current scanline
		R	SLN[15:8]								
		R	SLN[7:0]								
4F	DSTBY	W	0	0	1	1	0	1	0	0	Deep standby
		W	X	X	X	X	X	X	X	DSTBY	
51	WRDISBV	W	0	1	0	1	0	0	0	1	Write Display Brightness
		W	DBV[7:0]								
52	RDDISBV	W	0	1	0	1	0	0	1	0	Read Display Brightness Value
		R	DBV[7:0]								
53	WRCTRLD	W	0	1	0	1	0	0	1	1	Write CTRL Display
		W	X	X	BCTRL	X	DD	X	X	X	
54	RDCTRLD	W	0	1	0	1	0	0	1	1	Read Control Value Display-
		R	X	X	BCTRL	0	DD	0	0	0	
A1	RDDDB	W	1	0	1	0	0	0	0	1	Read the DDB from the provided location.
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
		R	x	x	x	x	x	x	x	x	
C4	DSPI	W	1	1	0	0	0	1	0	0	SPI interface setting for RAM write
		W	SPI_WRAM	X	DSPI_CFG[1:0]		DD	X	X	DSPI_EN	
DA	RDID1	W	1	1	0	1	1	0	1	0	Read ID1
		R	module's manufacturer[7:0]								
DB	RDID2	W	1	1	0	1	1	0	1	1	Read ID2
		R	LCD module/driver version [7:0]								
DC	RDID3	W	1	1	0	1	1	1	0	0	Read ID3

		R	LCD module/driver ID[7:0]

8.2. Command Description

8.2.1. NOP (00h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
NOP	W	00h	0000h	-	No Argument								
Description	This command does not have any effect on the display module. The NOP command may be used to terminate a Frame Memory Read or Frame Memory Write.												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart	

8.2.2. SWRESET: Software Reset (01h)

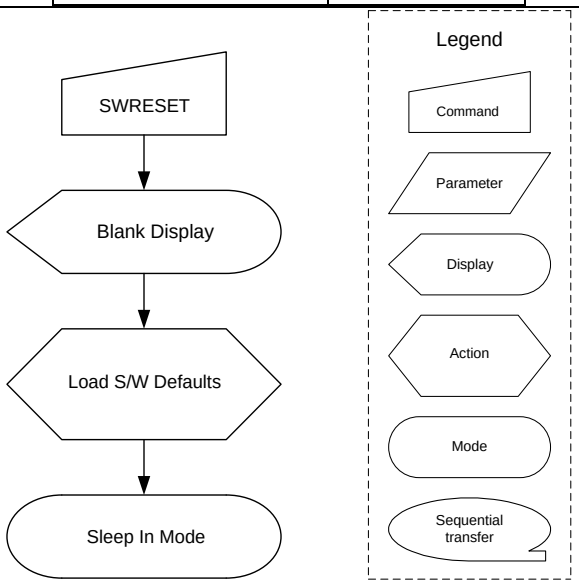
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SWRESET	W	01h	0100h	-	No Argument								
Description	The display module performs a software reset. Registers are written with their SW Reset default values. The Frame Memory contents are unaffected by this command												
Restriction	The host processor must wait 5 milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time. If a SWRESET is sent when the display module is in SLPIN Mode, the host processor must wait 120 milliseconds before sending an SLPOUT command. SWRESET should not be sent when the display module is not in SLPIN mode												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



8.2.3. RDDIDIF: Read display identification information (04h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDIDIF	R	04h	0400h	x	ID1[7:0]								96
			0401h	x	ID2[7:0]								13
			0402h	x	ID3[7:0]								00
Description	This read byte returns 24-bit display identification information. The 1st Parameter is dummy read. The 2nd parameter: AMOLED module's manufacturer ID. The 3rd parameter: AMOLED module/driver version ID The 4th parameter: AMOLED module/driver ID.												
Restriction	-												

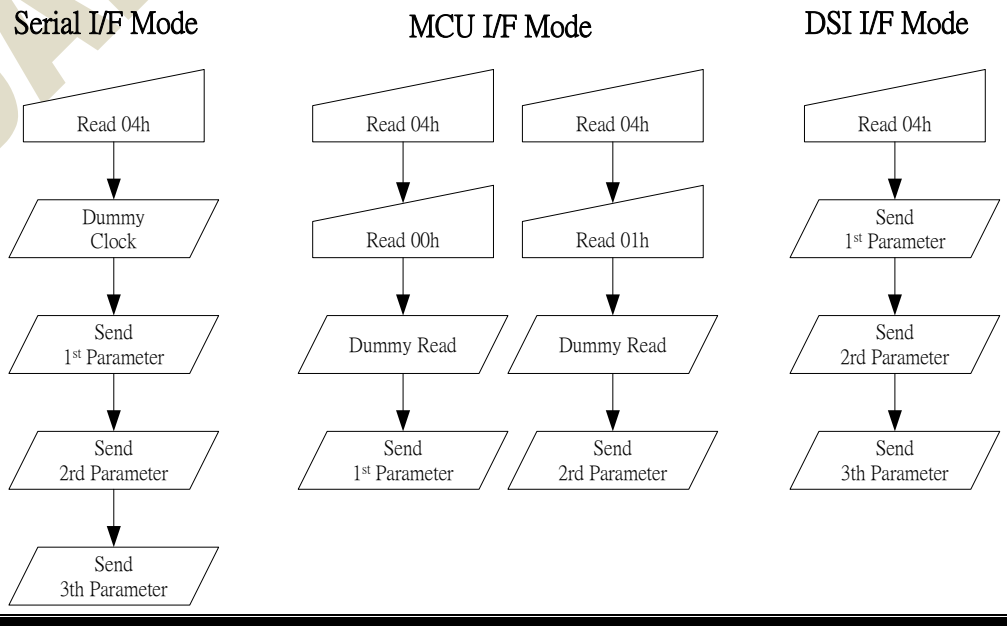
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	96h	13h	00h
SW Reset	96h	13h	00h
HW Reset	96h	13h	00h

Flow Chart



8.2.4. RDNUMPE: Read number of the parity errors (05h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDNUMPE	R	05h	0500h	-	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6:0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7:0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (=The read function is completed).												
Restriction	-												

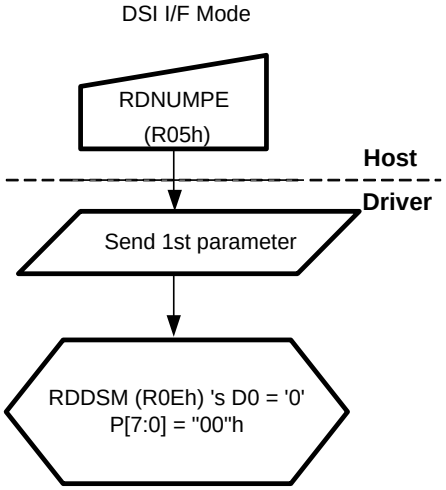
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

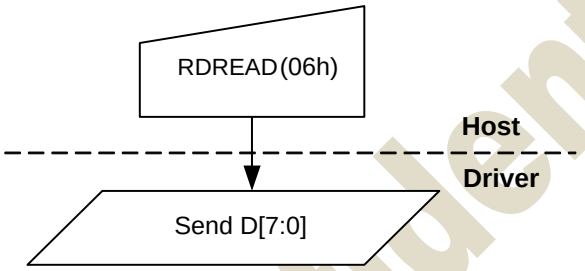
Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

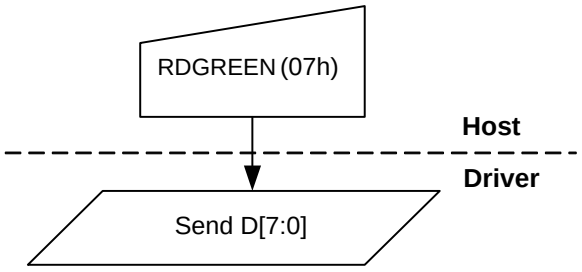
Flow Chart



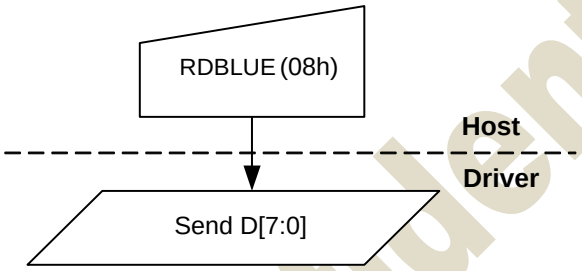
8.2.5. REDRD: Read Red Color (06h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
REDRD	R	06h	0600h	-	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	The first parameter is telling red color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'. 24 bit format: R7 is MSB and R0 is LSB. All bits are used.												
Restriction	-												
Flow Chart													

8.2.6. REDGREEN: Read Green Color (07h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
REDGREEN	R	07h	0700h	-	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	The first parameter is telling green color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. 18 bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'. 24 bit format: G7 is MSB and G0 is LSB. All bits are used.												
Restriction	-												
Flow Chart													

8.2.7. REDBLUE: Read Blue Color (08h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
REDBLUE	R	08h	0800h	-	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	The first parameter is telling blue color value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'. 24 bit format: B7 is MSB and B0 is LSB. All bits are used.												
Restriction	-												
Flow Chart													

8.2.8. RDDST: Read Display Status (09h)

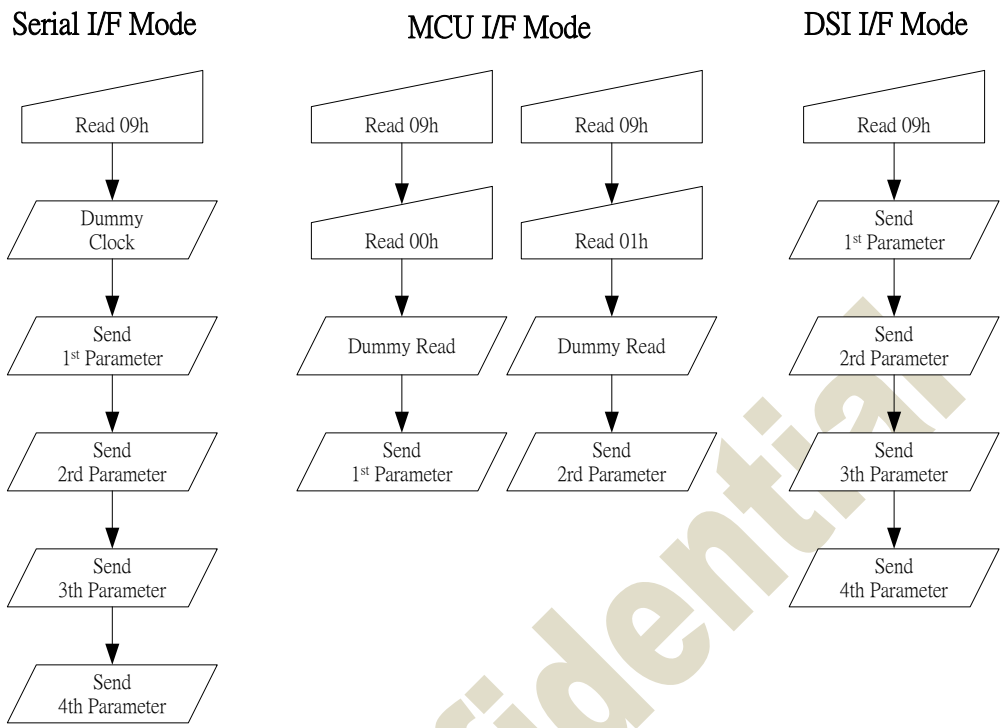
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDIDIF	R	09h	0900h	x	D[31:24]								-
			0901h	x	D[23:16]								-
			0902h	x	D[15:8]								-
			0903h	x	D[7:0]								-

Description

This command indicates the current status of the display as described in the table below

Bit	Description	Value
D31	Booster Voltage Status	'0' = Booster Off. '1' = Booster On.
D30	Page Address Order	'0' = Top to Bottom (MADCTL B7='0'). '1' = Bottom to Top (MADCTL B7='1').
D29	Column Address Order	'0' = Left to Right (MADCTL B6='0'). '1' = Right to Left (MADCTL B6='1')
D28	Page/Column Order	'0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').T
D27	Vertical Order	'0' = AMOLED Refresh Top to Bottom (When MADCTL B4='0'). '1' = AMOLED Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR Order	'0' = RGB (MADCTL B3='0'). '1' = BGR (MADCTL B3='1').
D25	Horizontal Order	'0' = AMOLED Refresh Left to Right (When MADCTL B2='0'). '1' = AMOLED Refresh Right to Left (When MADCTL B2='1').
D24	Flip Horizontal (SS)	'0' = Source driver scan direction Left to Right (When MADCTL B1='0'). '1' = Source driver scan direction Right to Left (When MADCTL B1='1').
D23	For Future Use	This bit is not applicable for this project, set it to '0'
D22 D21 D20	Interface Color Pixel Format Definition	Interface Format / D22 / D21 / D20: Not Defined 0 0 0 3 Bit /Pixel 0 1 1 8 Bit /Pixel 0 1 0 256 Gray /Pixel 0 0 1 Not Defined 1 0 0 16 Bit/Pixel 1 0 1 18 Bit/Pixel 1 1 0 24 Bit/Pixel 1 1 1
D19	Idle Mode On/Off	'0' = Idle Mode Off. '1' = Idle Mode On.
D18	Partial Mode On/Off	'0' = Partial Mode Off, '1' = Partial Mode On.
D17	Sleep In/Out	'0' = Sleep In Mode. '1' = Sleep Out Mode.
D16	Display Normal Mode On/Off	'0' = Partial or Scrolling Mode. '1' = Normal Mode.
D15	Vertical Scrolling Status	This bit is not applicable for this project, set it to '0'
D14	Horizontal Scrolling Status	This bit is not applicable for this project, set it to '0'
D13	Reserved	Reserved
D12	All Pixels On	'0' = Normal mode. '1' = All Pixels On.
D11	All Pixels Off	'0' = Normal mode. '1' = All Pixels Off.

<table>
<tr><td></td><td>
<table>
<tr><td>D10</td><td>Display On/Off</td><td>‘0’ = Display is Off.
‘1’ = Display is On.</td></tr>
<tr><td>D9</td><td>Tearing Effect Line On/Off</td><td>‘0’ =Tearing Effect Line Off.
‘1’ = Tearing Effect On.</td></tr>
<tr><td>D8
D7
D6</td><td>Gamma Curve Selection</td><td>
<table>
<tr><td>Gamma Curve Selected</td><td>B8</td><td>B7</td><td>B6</td></tr>
<tr><td>Gamma Curve 1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Gamma Curve 2</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Gamma Curve 3</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Gamma Curve 4</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td></tr>
<tr><td>D5</td><td>Tearing Effect Output Line Mode</td><td>‘0’ = Mode 1, V-Blanking only.
‘1’ = Mode 2, both H-Blanking and V-Blanking.</td></tr>
<tr><td>D4</td><td>Horizontal Sync. (HSYNC,DPI I/F)</td><td>This bit is not applicable for this project. set it to ‘0’</td></tr>
<tr><td>D3</td><td>Vertical Sync. (VSYNC,DPI I/F)</td><td>This bit is not applicable for this project. set it to ‘0’</td></tr>
<tr><td>D2</td><td>Pixel Clock (HSYNC,DPI I/F)</td><td>This bit is not applicable for this project. set it to ‘0’</td></tr>
<tr><td>D1</td><td>For Future Use</td><td>This bit is not applicable for this project. set it to ‘0’</td></tr>
<tr><td>D0</td><td>Parity Error on DSI</td><td>‘0’=No Parity Error.
‘1’=Parity Error.</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><td>D[31:24]</td><td>D[23:16]</td><td>D[15:8]</td><td>D[7:0]</td></tr>
<tr><td>Power On Sequence</td><td>0x00</td><td>0x71</td><td>0x00</td><td>0x00</td></tr>
<tr><td>SW Reset</td><td>0x00</td><td>0x71</td><td>0x00</td><td>0x00</td></tr>
<tr><td>HW Reset</td><td>0x00</td><td>0x71</td><td>0x00</td><td>0x00</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

8.2.9. RDDPM: Read Display Power Mode (0Ah)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDPM	R	0Ah	0A00h	-	D7	D6	D5	D4	D3	D2	D1	D0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	'0' = Booster Off. '1' = Booster On.
D6	Idle Mode On/Off	'0' = Idle Mode Off. '1' = Idle Mode On.
D5	Partial Mode On/Off	'0' = Partial Mode Off. '1' = Partial Mode On.
D4	Sleep In/Out	'0' = Sleep In Mode. '1' = Sleep Out Mode.
D3	Display Normal Mode On/Off	'0' = Display Normal Mode Off. '1' = Display Normal Mode On.
D2	Display On/Off	'0' = Display is Off. '1' = Display is On.
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Restriction

-

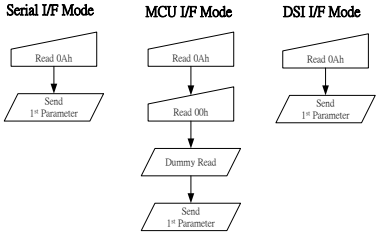
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



8.2.10.RDDMADCTL: Read Display MADCTL (0Bh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDMADCTL	R	0Bh	0B00h	-	D7	D6	D5	D4	D3	D2	D1	D0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Page Address Order (MY)	'0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1').
D6	Column Address Order (MX)	'0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1').
D5	Page/Column Order (MV)	'0' = Normal Mode (When MADCTL B5='0'). '1' = Reverse Mode (When MADCTL B5='1').
D4	Line Address Order	This bit is not applicable for this project. set it to '0'
D3	RGB/BGR Order	'0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').
D2	Display Data Latch Order	This bit is not applicable for this project. set it to '0'
D1	Source scan sequence	'0' = Source output Left to Right (When MADCTL B1='0'). '1' = Source output Right to Left (When MADCTL B1='1').
D0	Gate scan sequence	'0' = Gate output Top to Bottom (When MADCTL B1='0'). '1' = Gate output Bottom to Top (When MADCTL B1='1')

Restriction

-

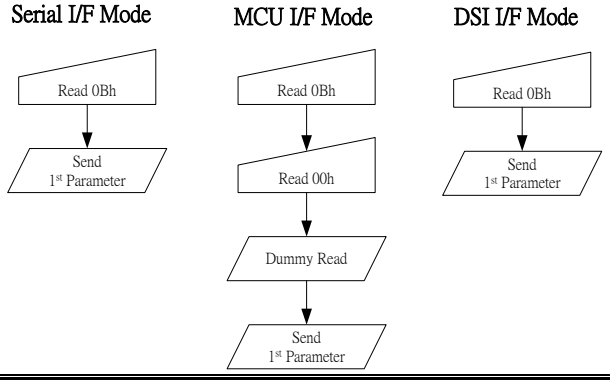
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

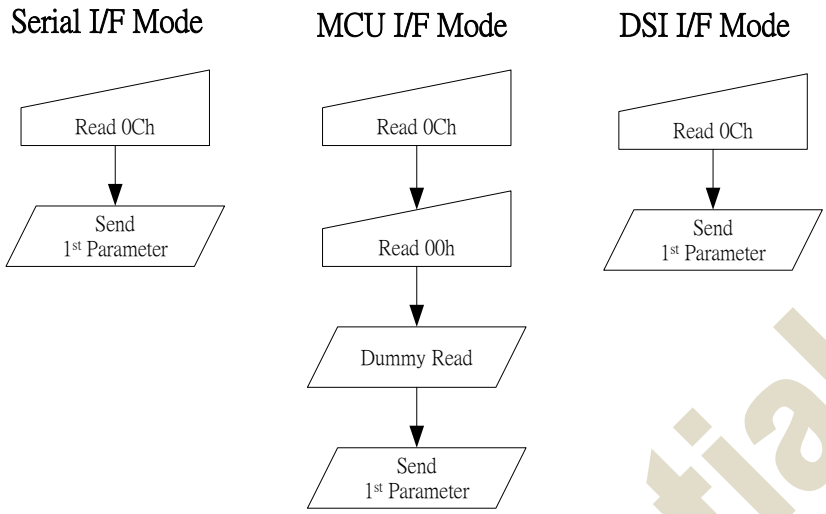
Status	Default Value
Power On Sequence	00h
SW Reset	No Change
HW Reset	00h

Flow Chart



8.2.11.RDDCOLMOD: Read Display Pixel Format (0Ch)

<table>
<tr><th rowspan="2">CMD/Pas</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th rowspan="2">D15-8</th><th rowspan="2">D7</th><th rowspan="2">D6</th><th rowspan="2">D5</th><th rowspan="2">D4</th><th rowspan="2">D3</th><th rowspan="2">D2</th><th rowspan="2">D1</th><th rowspan="2">D0</th><th rowspan="2">HEX</th></tr>
<tr><th>MIPI</th><th>Other</th></tr>
<tr><td>RDDCOLMOD</td><td>R</td><td>0Ch</td><td>0C00h</td><td>-</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td colspan="3">IFPF[2:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D6
D5
D4</td><td>DSI Interface Video mode Color Format (bypass ram mode)</td><td>‘101’ = 16 bits/pixel
‘110’ = 18 bits/pixel
‘111’ = 24 bits/pixel</td></tr>
<tr><td>D3</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D2
D1
D0</td><td>IFPF[2:0]
Control interface color format
(1) SPI/MPU/QSPI/DSI CMD mode
(2) DSI video mode access ram mode</td><td>‘001’ = SPI 1-1-1/pixel
‘010’ = SPI 3-3-2/pixel
‘011’ = SPI 256 Gray/pixel
‘101’ = 16 bits/pixel
‘110’ = 18 bits/pixel
‘111’ = 24 bits/pixel
Others are no define</td></tr>
</table>
Others are no define and invalid
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">When using DSI Video mode , the pixel color format is defined by the DSI video packet type. (not controlled by 0x3A CMD)
Ex: When the video packet type :0x3E – Packed pixel stream , 24-bit RGB, 8-8-8 Format , the read back color format is 3’b111=24 bits/pixel</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>06h (18 bits/pixel)</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>06h (18 bits/pixel)</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

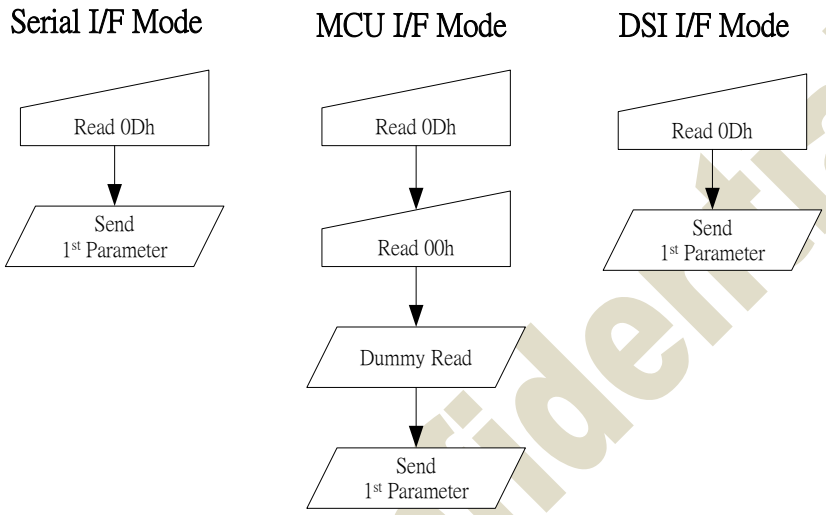
8.2.12.RDDIM: Read Display Image Mode (0Dh)

<table>
<tr><th rowspan="2">CMD/Pas</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th rowspan="2">D15-8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th rowspan="2">HEX</th></tr>
<tr><th>MIPI</th><th>Other</th></tr>
<tr><td>RDDIM</td><td>R</td><td>0Dh</td><td>0D00h</td><td>-</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>Vertical Scrolling On/Off</td><td>This bit is not applicable for this project, set it to ‘0’</td></tr>
<tr><td>D6</td><td>Horizontal Scrolling Status</td><td>This bit is not applicable for this project, set it to ‘0’</td></tr>
<tr><td>D5</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>D4</td><td>All Pixels On</td><td>‘0’ = Normal Display
‘1’ = White Display</td></tr>
<tr><td>D3</td><td>All Pixels Off</td><td>‘0’ = Normal Display
‘1’ = Black Display</td></tr>
<tr><td>D2
D1
D0</td><td>Gamma Curve Selection</td><td>
<table>
<tr><th>Gamma Curve Selected</th><th>D2</th><th>D1</th><th>D0</th><th>Gamma Set (26h)</th></tr>
<tr><td>Gamma Curve 1</td><td>0</td><td>0</td><td>0</td><td>CG0</td></tr>
<tr><td>Gamma Curve 2</td><td>0</td><td>0</td><td>1</td><td>CG1</td></tr>
<tr><td>Gamma Curve 3</td><td>0</td><td>1</td><td>0</td><td>CG2</td></tr>
<tr><td>Gamma Curve 4</td><td>0</td><td>1</td><td>1</td><td>CG3</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td><td></td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>1</td><td></td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>0</td><td></td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>1</td><td></td></tr>
</table>
</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.13. RDDSM: Read Display Signal Mode (0Eh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDSM	R	0Eh	0E00h	-	TEON	TEM	0	0	0	0	0	D0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	'0' = Tearing Effect Line Off. '1' = Tearing Effect On.
D6	Tearing Effect Line Mode	'0' = Mode 1. '1' = Mode 2.
D5	Horizontal Sync. On/Off.	This bit is not applicable for this project, set it to '0'
D4	Vertical Sync. On/Off.	This bit is not applicable for this project, set it to '0'
D3	Pixel Clock(PCLK) On/Off.	This bit is not applicable for this project, set it to '0'
D2	Data Enable(DE) On/Off.	This bit is not applicable for this project, set it to '0'
D1	Not Defined	For future use and are set to '0'.
D0	Parity Error on DSI	'0'=No Parity Error. '1'=Parity Error.

Restriction

-

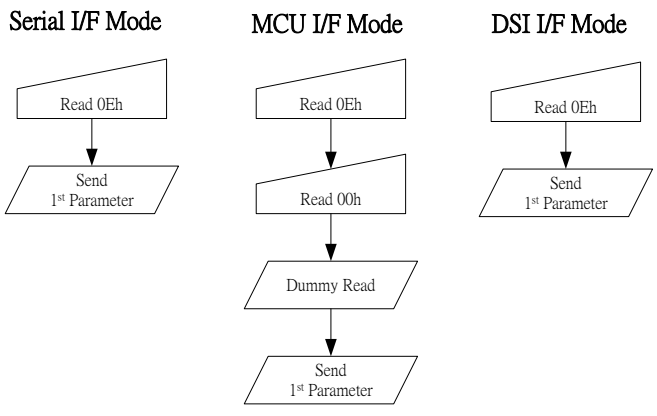
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.14. RDDSDR: Read Display Self-Diagnostic Result (0Fh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDSDR	R	0Fh	0F00h	-	D7	D6	D5	D4	0	0	0	0	-

Description

The display module returns the self-diagnostic results following a SLPOUT command. self-diagnostic functions is list as below.

Bit	Description	Value
D7	Register Loading Detection	See section “Sleep Out –command and self-diagnostic functions of the display module”
D6	Functionality Detection	
D5	Chip Attachment Detection	Set to ‘0’ if feature unimplemented.
D4	Display Glass Break Detection	Set to ‘0’ if feature unimplemented.
D3	Reserved	Set to ‘0’.
D2		Set to ‘0’.
D1		Set to ‘0’.
D0		Set to ‘0’.

Restriction

-

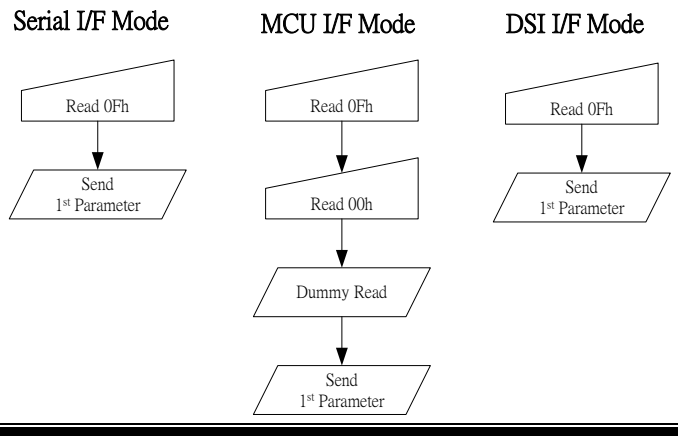
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

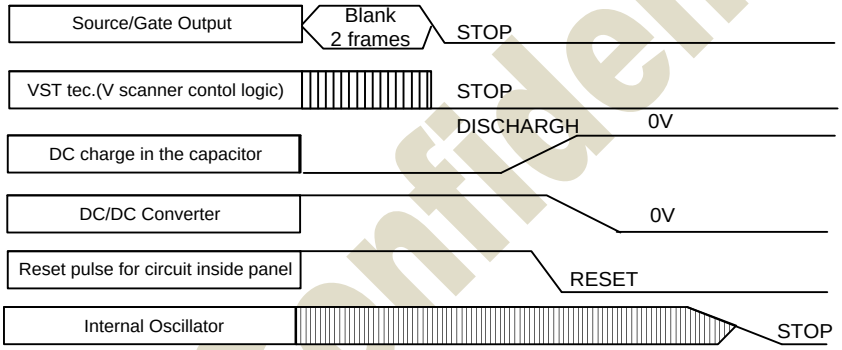
Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

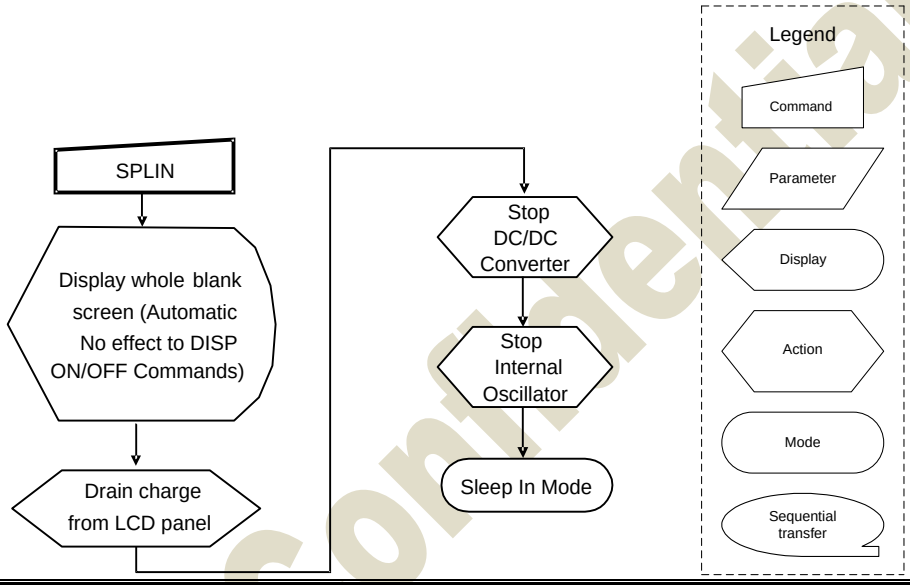
Flow Chart



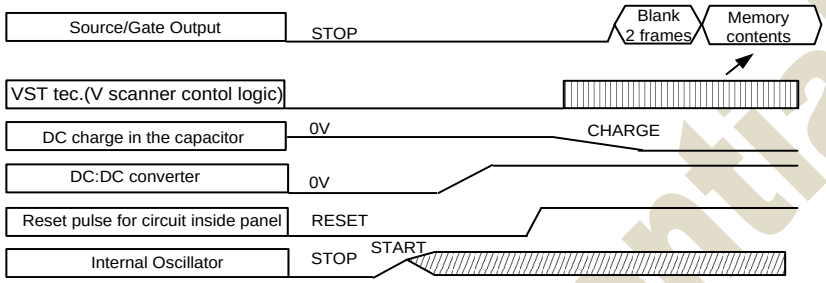
8.2.15. SLPIN: Sleep In (10h)

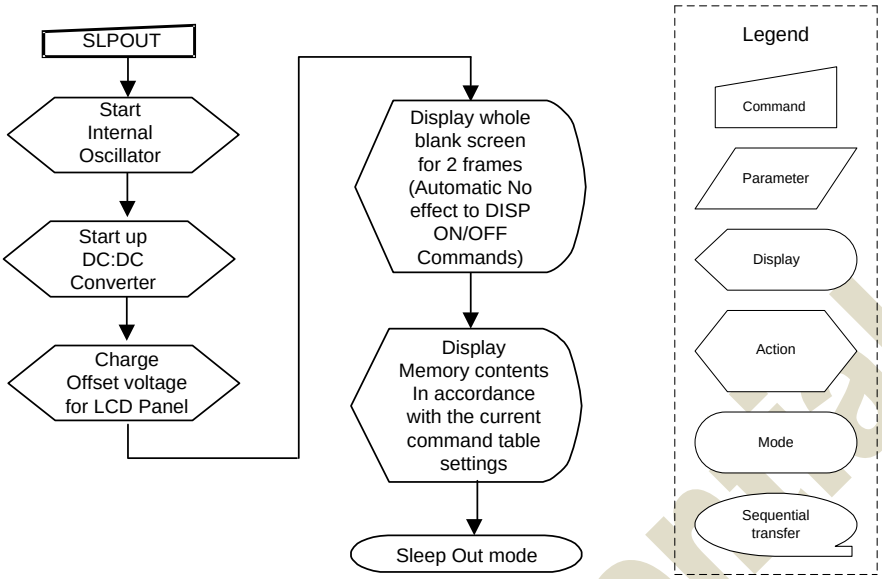
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SLPIN	W	10h	1000h	-	No Argument								
Description	This command causes the AMOLED module to enter the minimum power consumption mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest power mode the display module supports. MCU interface and memory are still working and the memory keeps its contents. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  											
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>SW Reset</td><td>Sleep in mode</td></tr><tr><td>HW Reset</td><td>Sleep in mode</td></tr></table>
Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued. 

8.2.16. SLPOUT: Sleep Out (11h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
SLPOUT	W	11h	1100h	-	No Argument								
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep in mode</td></tr><tr><td>SW Reset</td><td>Sleep in mode</td></tr><tr><td>HW Reset</td><td>Sleep in mode</td></tr></table>												

Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued. 

8.2.17. PTLON: Partial Mode ON (12h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PTLON	W	**12h**	**1200h**	-	No Argument								
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.												
Restriction	This command has no effect when Partial mode is active.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
SW Reset	Normal Mode On
HW Reset	Normal Mode On

Flow Chart	See Partial Area (30h)

8.2.18. NORON: Normal Display Mode ON (13h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
NORON	W	13h	1300h	-	No Argument								
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off. There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
SW Reset	Normal Mode On
HW Reset	Normal Mode On

Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.

8.2.19. RDCUSTM_ID: Read Customer ID (1Bh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDCUSTM_ID	R	22h	1B00h	x	CUSTM_ID1[7:0]								
			1B01h		CUSTM_ID2[7:0]								
			..	x	..								
			1B0Fh	x	CUSTM_ID16[7:0]								
			1B00h	x	CUSTM_ID1[7:0]								
Description	This read byte returns display manufacturer identification information.												
Restriction	-												

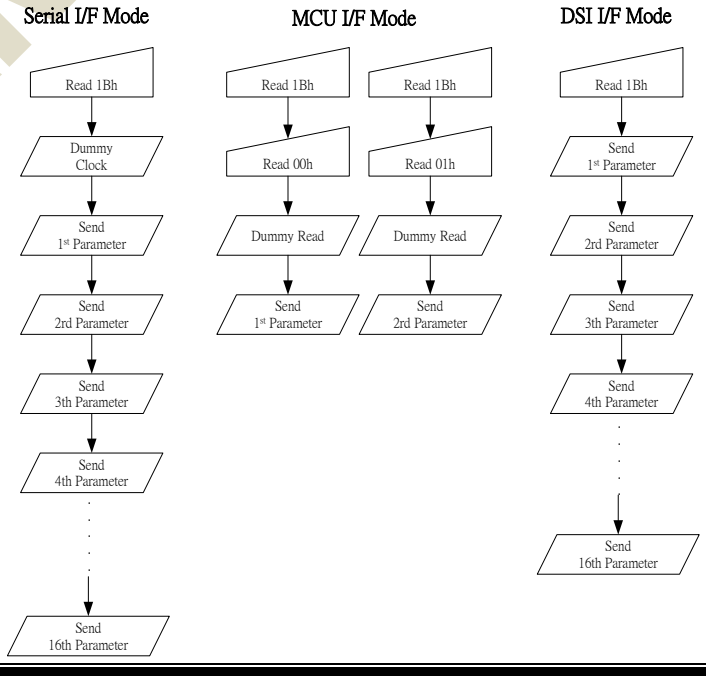
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CUSTM_ID0 ~ CUSTM_ID15
Power On Sequence	
SW Reset	
HW Reset	

Flow Chart



8.2.20. ALLPOFF: All Pixel Off (22h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
ALLPOFF	W	22h	2200h	-	No Argument								

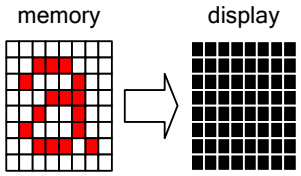
Description

This command turns the display panel black in ‘Sleep Out’ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’.

This command makes no change of contents of frame memory.

This command does not change any other status

(Example)



‘All Pixels On’, ’Normal Display Mode On’ or ’Partial Mode On’ – commands are used to leave this mode. The display panel is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ -commands

Restriction

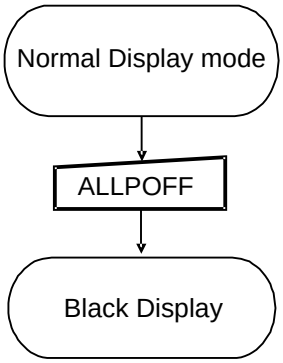
This command has no effect when module is already in All Pixel Off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Flow Chart



8.2.21.ALLPON: All Pixel On (23h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
ALLPON	W	23h	2300h	-	No Argument								-

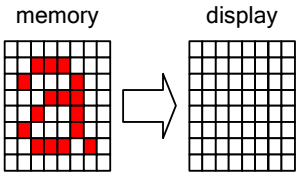
Description

This command turns the display panel white in ‘Sleep out ‘ –mode and a status of the ‘Display On/Off’ –register can be ‘on’ or ‘off’.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



‘All Pixels Off’, ’Normal Display Mode On’ or ’Partial Mode On’ – commands are used to leave this mode. The display is showing the content of the frame memory after ‘Normal Display Mode On’ and ‘Partial Mode On’ –commands.

Restriction

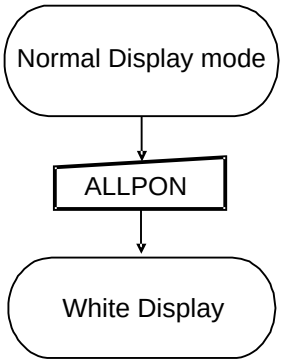
This command has no effect when module is already in All Pixel ON mode.

Register Availability

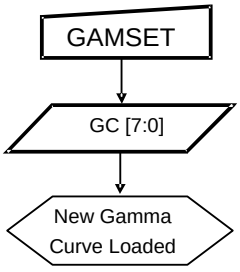
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Flow Chart



8.2.22. GAMSET: Gamma Set (26h)

<table>
<tr><th rowspan="2">CMD/Pas</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th rowspan="2">D15-8</th><th rowspan="2">D7</th><th rowspan="2">D6</th><th rowspan="2">D5</th><th rowspan="2">D4</th><th rowspan="2">D3</th><th rowspan="2">D2</th><th rowspan="2">D1</th><th rowspan="2">D0</th><th rowspan="2">HEX</th></tr>
<tr><th>MIPI</th><th>Other</th></tr>
<tr><td>GAMSET</td><td>W</td><td>26h</td><td>2600h</td><td>-</td><td colspan="8">GC[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:
<table>
<tr><th>GC[7..0]</th><th>Parameter</th><th>Curve selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr>
<tr><td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr>
<tr><td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr>
<tr><td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr>
</table>
Note: All other values are undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>SW Reset</td><td>01h</td></tr>
<tr><td>HW Reset</td><td>01h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

8.2.23. DISPOFF: Display Off (28h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DISPOFF	W	28h	2600h	-	No Argument								
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.												
Restriction	This command has no effect when module is already in display off mode.												

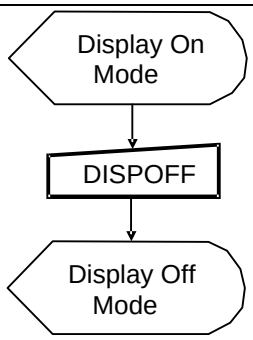
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
SW Reset	Display off
HW Reset	Display off

Flow Chart



8.2.24. DISPON: Display On (29h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DISPON	W	29h	2900h	-	No Argument								
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status.												
Restriction	This command has no effect when module is already in display on mode.												

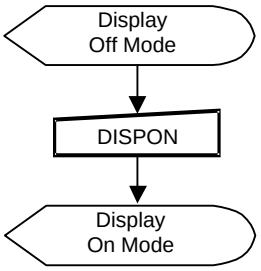
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

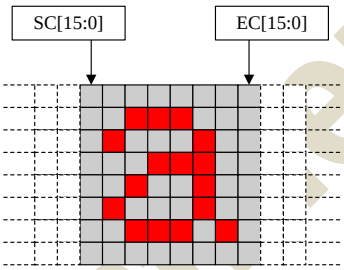
Default

Status	Default Value
Power On Sequence	Display off
SW Reset	Display off
HW Reset	Display off

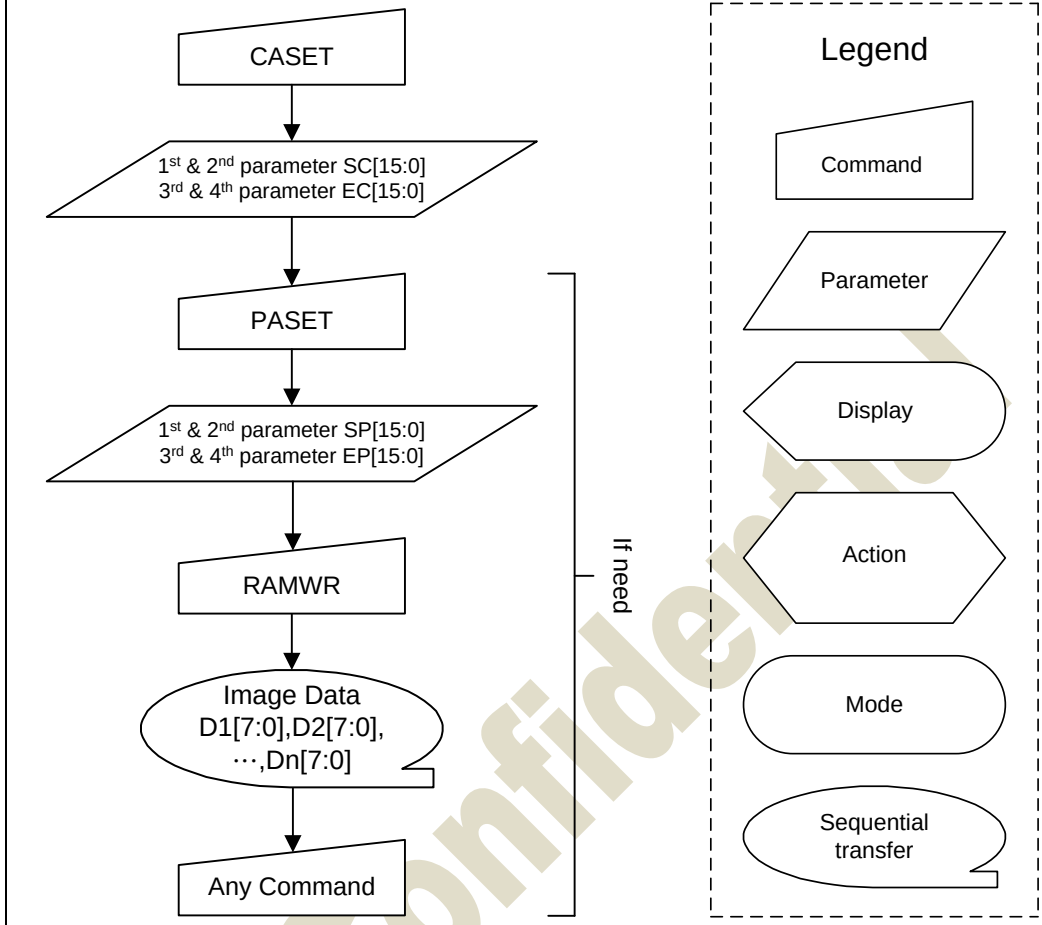
Flow Chart



8.2.25.CASET: Column Address Set (2Ah)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
CASET	W	2Ah	2A00h	-	SC[15:8]								00
			2A01h	-	SC[7:0]								00
			2A02h	-	EC[15:8]								00
			2A03h	-	EC[7:0]								EF
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.  												
Restriction	(1) SC[15:0] always must be equal to or less than EC[15:0] (2) The SC[15:0] and EC[15:0]-SC[15:0]+1 must can be divided by 2. Note 1: When SC[15:0] or EC[15:0] is greater than EFh (when MADCTL's B5=0) or 18Fh (when MADCTL's B5=1), data of out of range will be ignored												
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>												
Default	<table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC[15:0] = 0000h</td><td>EC[15:0] = 00EFh</td></tr><tr><td>SW Reset</td><td>SC[15:0] = 0000h</td><td>When MV=0: EC[15:0] = 00EFh When MV=1: EC[15:0] = 013Fh</td></tr><tr><td>HW Reset</td><td>SC[15:0] = 0000h</td><td>EC[15:0] = 00EFh</td></tr></table>												

Flow Chart



8.2.26.PASET: Page Address Set (2Bh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PASET	W	2Bh	2B00h	-	SP[15:8]								00
			2B01h	-	SP[7:0]								00
			2B02h	-	EP[15:8]								01
			2B03h	-	EP[7:0]								8F

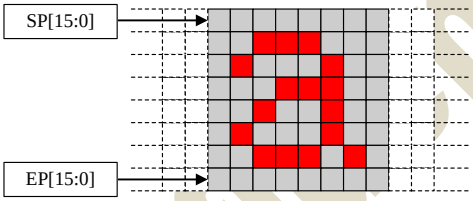
Description

This command is used to define area of frame memory where MCU can access.

This command makes no change on the other driver status.

The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.

Each value represents one Page line in the Frame Memory.



Restriction

(1) SP[15:0] always must be equal to or less than EP[15:0]

(2) The SP[15:0] and EP[15:0] – SP[15:0]+1 must can be divided by 2.

Note 1: When SP[15:0] or EP[15:0] is greater than 18Fh (When MADCTL's B5=0) or EFh (When MADCTL's B5=1), data of out of range will be ignored.

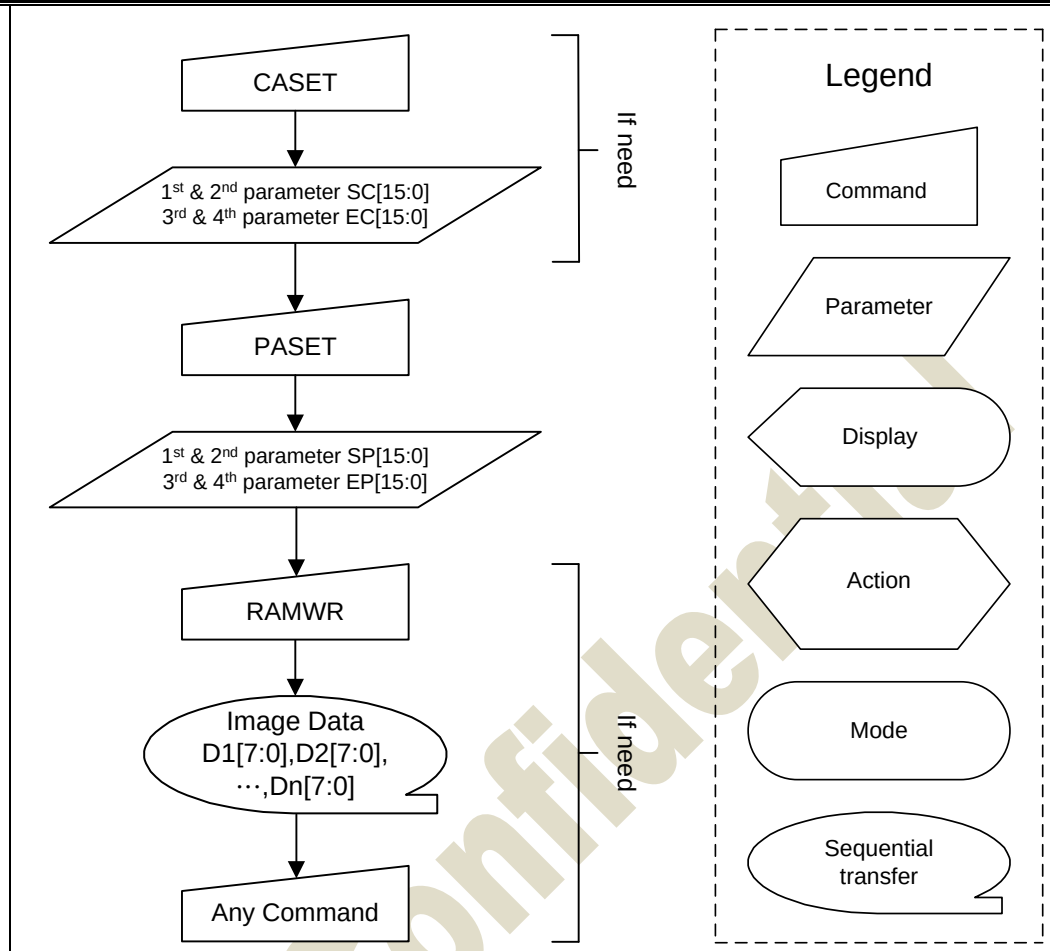
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0] = 0000h	EC[15:0] = 013Fh
SW Reset	SP[15:0] = 0000h	When MV=0: EC[15:0] = 013Fh When MV=1: EC[15:0] = 00EFh
HW Reset	SP[15:0] = 0000h	EC[15:0] = 013Fh

Flow Chart



8.2.27. RAMWR: Memory Write (2Ch)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RAMWR	W	2Ch	2C00h	-	0	0	1	0	1	1	0	0	2C
			1st Pixel	-	D1								
			.	-	.								
			Nth Pixel	-	Dn								

Description

This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting.
Then D[17:0] is stored in frame memory and the column register and the page register Incremented.
Sending any other command can stop frame Write.

Restriction

In all color modes, there is no restriction on length of parameters..

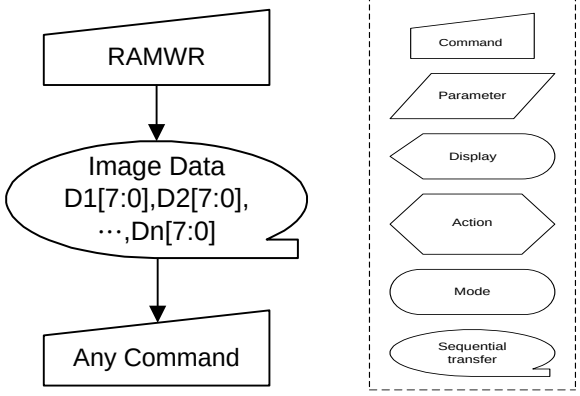
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



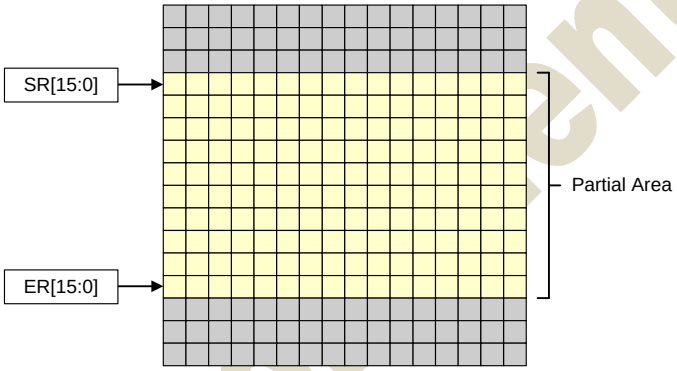
8.2.28. PTLAR: Partial Area (30h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
PTLAR	W	30h	3000h	-	SR[15:8]								00
			3001h	-	SR[7:0]								00
			3002h	-	ER[15:8]								01
			3003h	-	ER[7:0]								8F

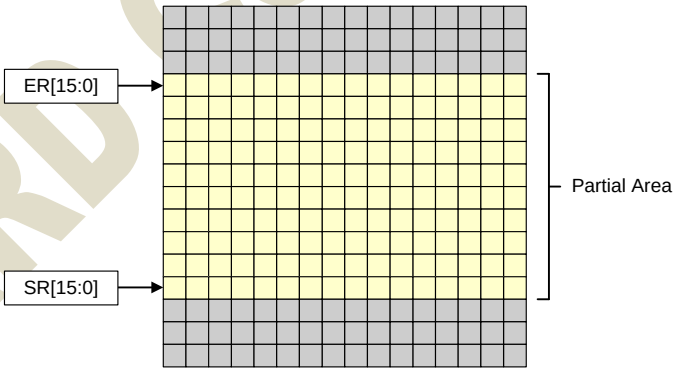
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

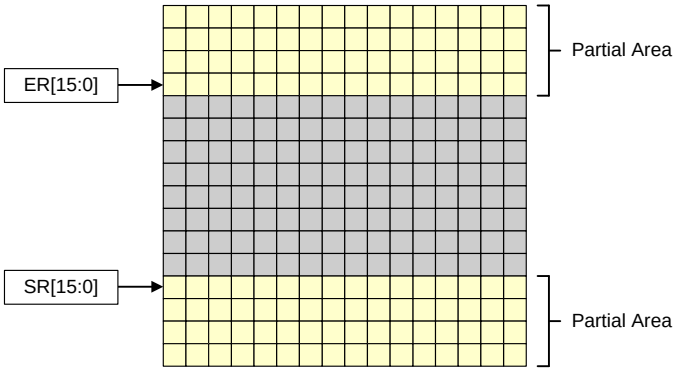
If End Row>Start Row when MADCTL B4 (ML) = 0:



If End Row>Start Row when MADCTL B4 (ML) = 1:



If End Row<Start Row when MADCTL B4=0:



If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR[15..0] and ER[15..0] setting should be within max available Display Area..

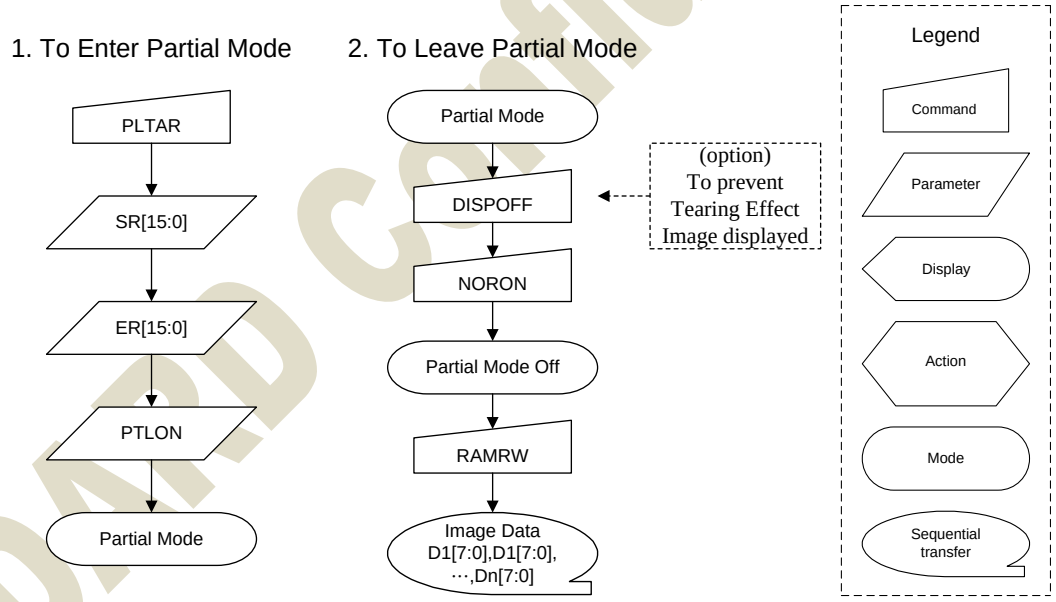
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

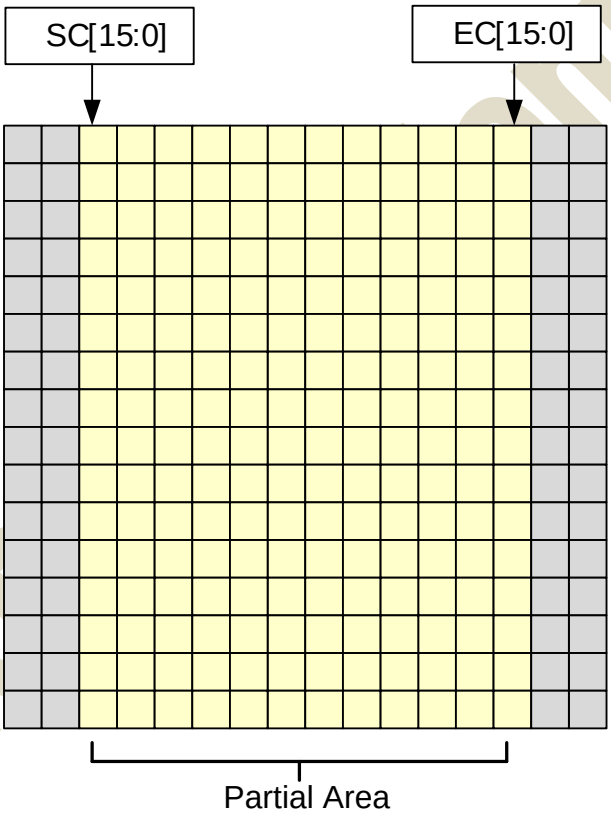
Default

Status	Default Value	
Power On Sequence	SR[15:0] = 0000h	ER[15:0] = 018Fh
SW Reset	SR[15:0] = 0000h	ER[15:0] = 018Fh
HW Reset	SR[15:0] = 0000h	ER[15:0] = 018Fh

Flow Chart



8.2.29. Vertical PTLAR: Vertical Partial Area (31h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
Vertical PTLAR	W	31h	3100h	-	PSC[15:8]								00
			3101h	-	PSC[7:0]								00
			3102h	-	PEC[15:8]								00
			3103h	-	PEC[7:0]								EF
Description	This command defines the Vertical Partial Display mode's display area. There are two parameters associated with this command , the first defines the Start column(SC) and the second the End Column(EC), as illustrated in the following figure.: 												
Restriction	SC[15..0] and EC[15..0] setting should be within max available Display Area..												
Register Availability													

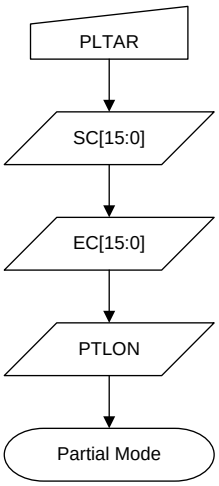
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

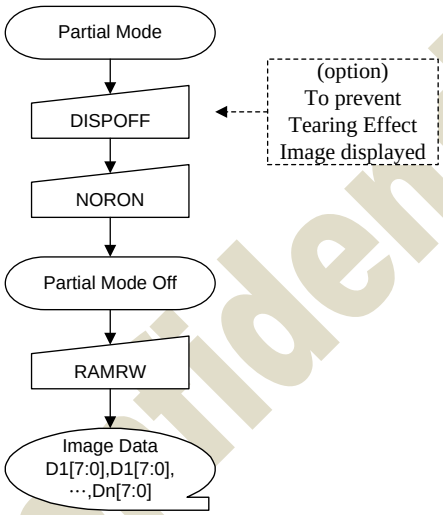
Status	Default Value	
Power On Sequence	SC[15:0] = 0000h	EC[15:0] = 0EFh
SW Reset	SC[15:0] = 0000h	EC[15:0] = 0EFh
HW Reset	SC[15:0] = 0000h	EC[15:0] = 0EFh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.30.TEOFF: Tearing Effect Line OFF (34h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
TEOFF	W	34h	3400h	-	No Argument								
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

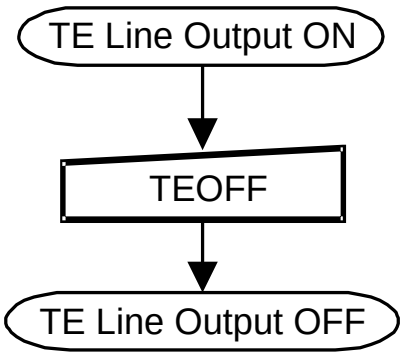
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart



8.2.31.TEON: Tearing Effect Line ON (35h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
TEON	W	35h	3500h	-	-	-	-	-	-	-	-	M	00

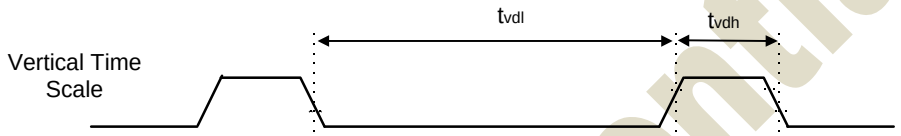
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

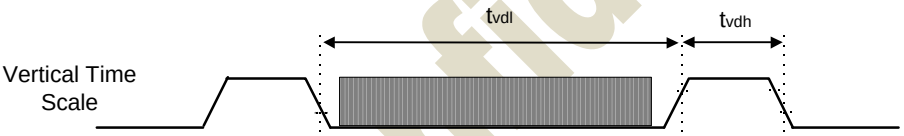
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

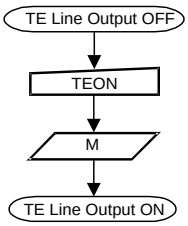
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
SW Reset	Off
HW Reset	Off

Flow Chart



8.2.32. MADCTL: Memory Access Control(36h)

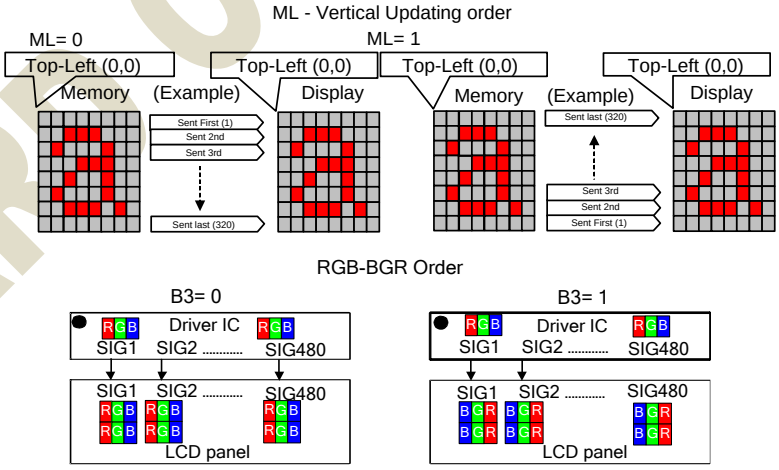
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
MADCTL	W	36h	3600h	-	D7	D6	D5	D4	D3	D2	D1	D0	-

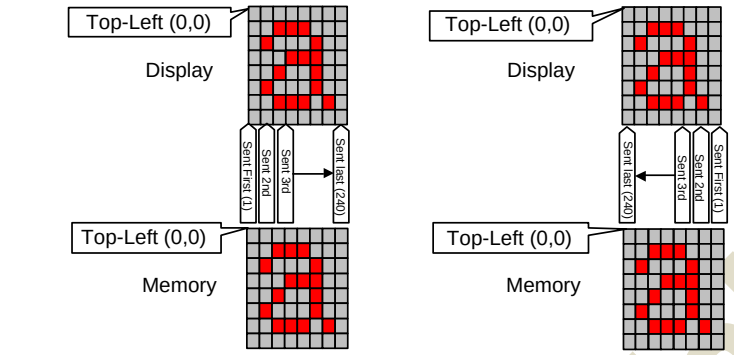
Description

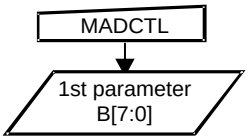
This command defines read/ write scanning direction of frame memory.

This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Reserved	
B3	RGB-BGR ORDER (BGR)	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
B2	Reserved	
B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module
B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module



<table>
<tr><td></td><td>
MH - Horizontal Updating order
MH= 0 MH= 1


Note: Top-Left (0,0) means a physical memory location
</td></tr>
<tr><td>Restriction</td><td>D1 and D0 are set to ‘00’ internally.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

8.2.33. IDMOFF: Idle Mode OFF (38h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
IDMOFF	W	38h	3800h	-	No Argument								00
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on.												
Restriction	This command has no effect when module is already in idle off mode.												

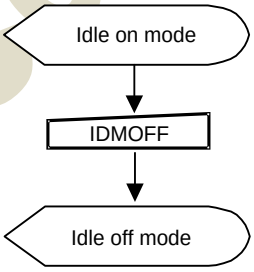
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode off
SW Reset	Idle mode off
HW Reset	Idle mode off

Flow Chart



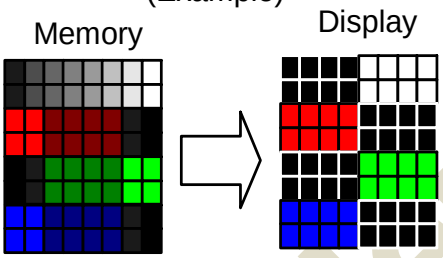
8.2.34. IDMON: Idle Mode ON (39h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
IDMON	W	39h	3900h	-	No Argument								

Description

This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

(Example)



Color	$R_5R_4R_3R_2R_1R_0$	$G_5G_4G_3G_2G_1G_0$	$B_5B_4B_3B_2B_1B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

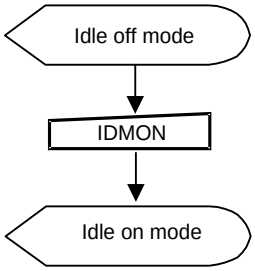
This command has no effect when module is already in idle on mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

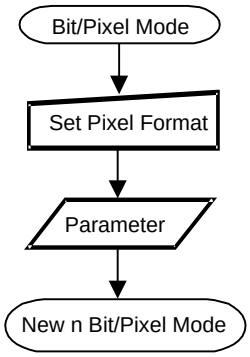
Default

Status	Default Value
Power On Sequence	Idle mode off
SW Reset	Idle mode off
HW Reset	Idle mode off

Flow Chart	

8.2.35. COLMOD: Pixel Format Set (3Ah)

<table>
<tr><th rowspan="2">CMD/Pas</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th rowspan="2">D15-8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th rowspan="2">HEX</th></tr>
<tr><th>MIPI</th><th>Other</th><th>0</th><th>0</th><th>0</th><th>0</th><th>0</th><th colspan="3">IFPF[2:0]</th></tr>
<tr><td>COLMOD</td><td>W</td><td>3Ah</td><td>3A00h</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">IFPF[2:0]</td><td>07</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define the pixel format of RGB picture data, which is to be transferred via interface
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td>D7</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D6
D5
D4</td><td>DSI Interface Video mode Color Format (bypass ram mode)</td><td>‘101’ = 16 bits/pixel
‘110’ = 18 bits/pixel
‘111’ = 24 bits/pixel</td></tr>
<tr><td>D3</td><td>-</td><td>Set to ‘0’</td></tr>
<tr><td>D2
D1
D0</td><td>IFPF[2:0]
Control interface color format
(3) SPI/MPU/QSPI/DSI CMD mode
(4) DSI video mode access ram mode</td><td>‘001’ = SPI 1-1-1/pixel
‘010’ = SPI 3-3-2/pixel
‘011’ = SPI 256 Gray/pixel
‘101’ = 16 bits/pixel
‘110’ = 18 bits/pixel
‘111’ = 24 bits/pixel
Others are no define</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">DSI CMD mode only support 16bits/pixel 18bits/pixel and 24 bits/pixel.</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24bits/pixel</td></tr>
<tr><td>SW Reset</td><td>24bits/pixel</td></tr>
<tr><td>HW Reset</td><td>24bits/pixel</td></tr>
</table></td></tr>
</table>

Flow Chart	

8.2.36. WRMEMC: Write Memory Continue (3Ch)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRMEMC	W	3Ch	3C00h	-	0	0	1	1	1	1	0	0	3C
			1st Pixel	-	D1								
			.	-	.								
			Nth Pixel	-	Dn								
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous Write Memory Continue (3Ch) or Memory Write Start (2Ch) command. Sending any other command can stop frame Write. If MATCDL MV = 0: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. If MATCDL MV = 1: Data is written continuing from the pixel location after the write range of the previous Memory Write Start (2Ch) or Write Memory Continue (3Ch). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.												
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.												

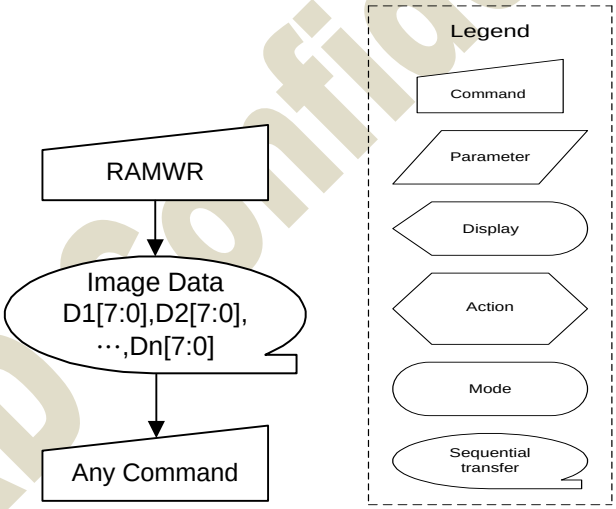
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.37. STESL: Set Tear Scan line (44h)

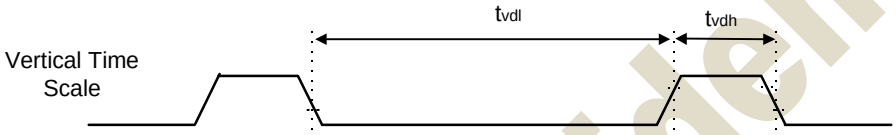
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
STESL	W	44h	4400h	-	TELINE[15:8]								
			4401h	-	TELINE[7:0]								

Description

This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELINE. The TE signal is not affected by changing MADCTL bit B4.

The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

The Tearing Effect Output line consists of V-Blanking information only:



Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.

Restriction

A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.

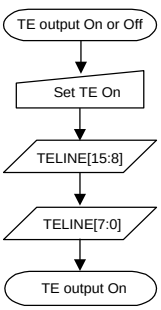
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
SW Reset	0000h
HW Reset	0000h

Flow Chart



8.2.38. GSCAN: Get Scan line (45h)

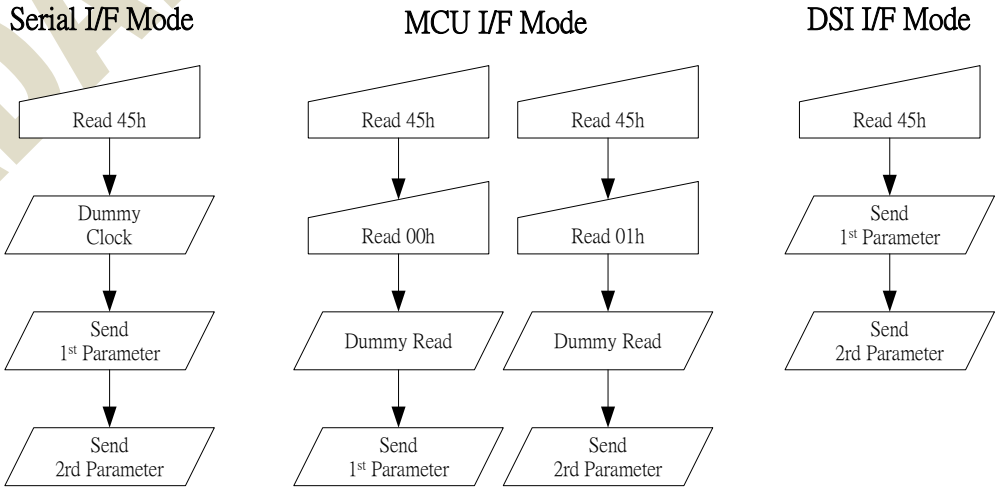
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
GSCAN	R	45h	4500h	-	SLN[15:8]								
			4501h	-	SLN [7:0]								
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get scanline is undefined.												
Restriction	-												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

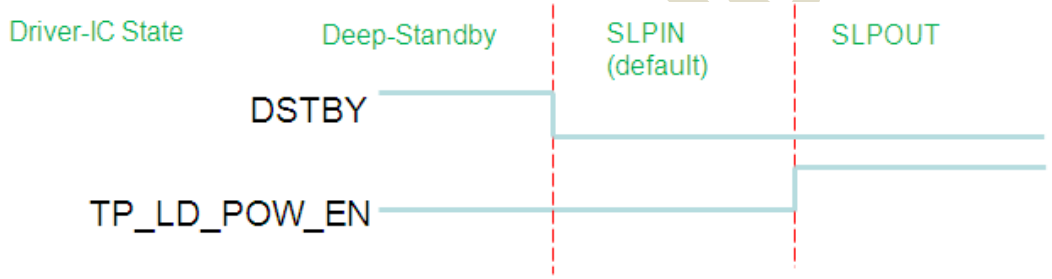
Default

Status	Default Value
Power On Sequence	0000h
SW Reset	0000h
HW Reset	0000h

Flow Chart



8.2.39. POWER STATE: Power status setting (4Fh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
DSTBON	W	4Fh	4F00h	-	0	0	0	0	0	0	0	DSTBY	
Description	This command is used to set power state. **DSTBY:** Standby mode select. DSTBY=1, driver IC enters the deep standby mode when POW_EN=0. DSTBY=0, driver IC enters the standby mode when POW_EN=0. Driver IC Can write DSTBY register in SLPIN state and then enter into Deep Standby state. User can't write DSTBY register when Driver IC in SLPOUT state or Display-On. When DSTBY=1, all the display operation stops, All the internal operations and R-C oscillators are suspended. Host need pull reset pin to low pulse more than 3ms, DDI will exist deep standby mode.  												
Restriction	-												

8.2.40. WRDISBV: Write Display Brightness (51h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRDISBV	W	51h	5100h	-	DBV[7:0]								00
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “Content adaptive brightness control (CABC) function”												
Restriction	-												

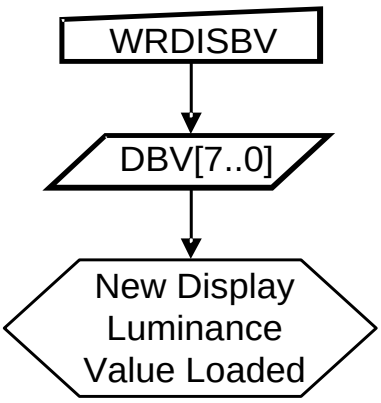
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.41. RDDISBV: Read Display Brightness Value (52h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDISBV	R	52h	5200h	-	DBV[7:0]								

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is '0' when bit BCTRL of Write CTRL Display (53h)" command is '0'.

DBV[7:0] is manual set brightness specified with Write CTRL Display (53h)" command when bit BCTRL is '1'.

Restriction

-

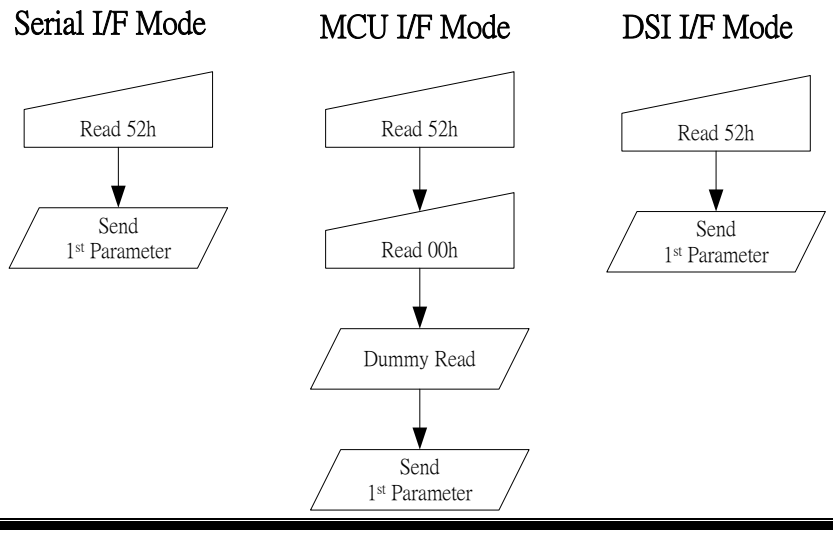
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.42. WRCTRLD: Write CTRL Display (53h)

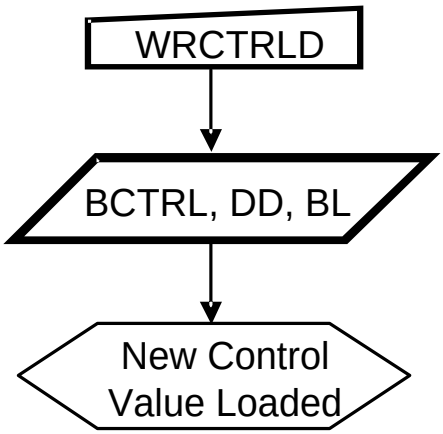
CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRCTRLD	W	53h	5300h	-	0	0	BCTRL	0	DD	0	0	0	00
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on												
Restriction	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart	

8.2.43. RDCTRLD: Read CTRL Value Display (54h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDCTRLD	W	54h	5400h	-	0	0	BCTRL	0	DD	0	0	0	00

Description

This command returns ambient light and brightness control values.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off

1 = On

Display Dimming (DD):

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

Restriction

-

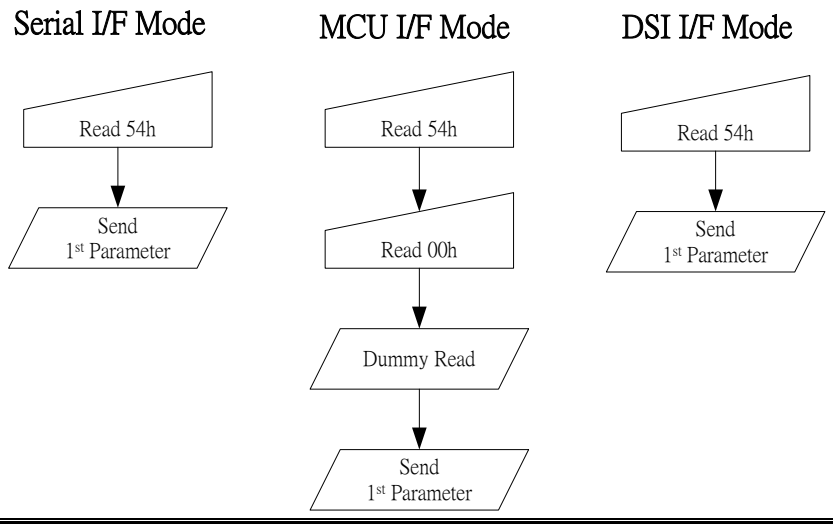
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

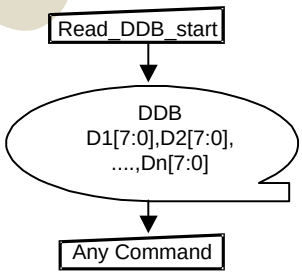
Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.44. RDDDB: Read DDB Start (A1h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDDDB	R	A1h	A100h	-	DDB_DATA1								
			A101h		DDB_DAT2								
			A102h	-	DDB_DAT3								
Description	This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns 3 bytes data. The format of returned data is as follows: Parameter 1: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 2: MS (most significant) byte of Supplier ID. Parameter 3: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.												
Restriction	-												
Flow Chart													

8.2.45. SetDSPIMode: set_DSPI mode (C4h)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRACL	W	C4h	C400h	-	SPI_WRAM	0	DSPI_CFG[1:0]		0	0	0	DSPI_EN	00

Description

Bit	Description	value
SPI_WRAM	This command is used in SPI interfaces. Making sure to set SPI_WRAM=1 before host writes SRAM via SPI interfaces.	0: disable 1: SPI interface write RAM enable
DSPI_CFG[1:0]	Dual SPI MODE Selection	00: 1P1T for 1 wire 10: 1P1T for 2 wire 11: 2P3T for 2 wire 01: reserved
DSPI_EN	DUAL SPI MODE Enable	0: disable 1: enable

Restriction

-

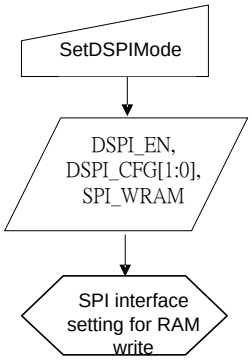
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



8.2.46. RDID1: Read ID1 (DAh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDID1	R	DAh	DA00h	-	ID1[7:0]								-
Description	This read byte identifies the AMOLED module's manufacturer.												
Restriction	-												

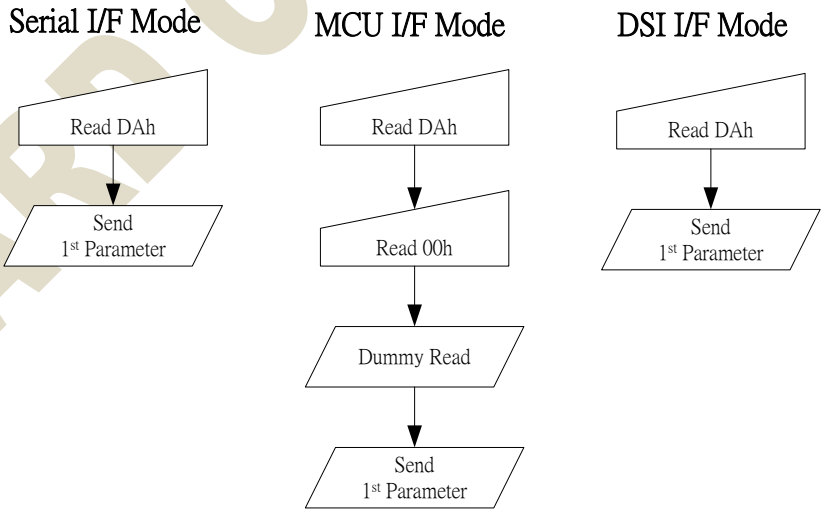
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	91h
SW Reset	91h
HW Reset	91h

Flow Chart



8.2.47. RDID2: Read ID2 (DBh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDID2	R	DBh	DB00h	-	ID2[7:0]								-
Description	This read byte is used to track the AMOLED module/driver version.												
Restriction	-												

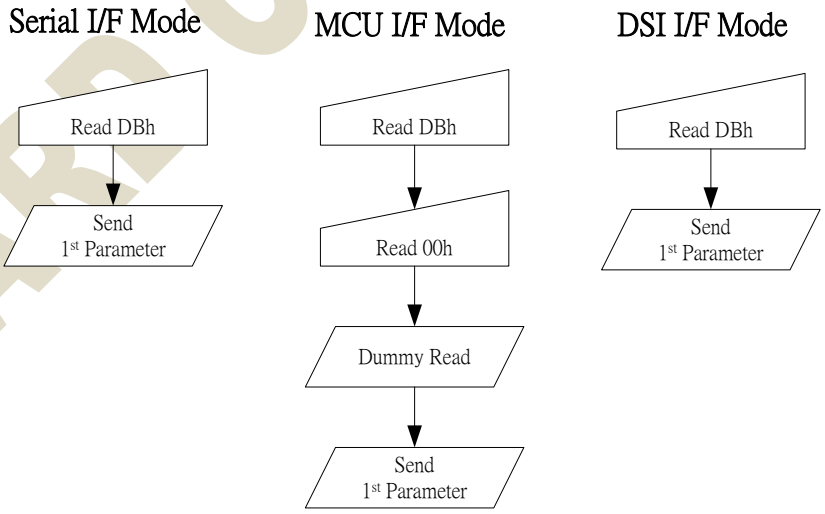
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	63h
SW Reset	63h
HW Reset	63h

Flow Chart



8.2.48. RDID3: Read ID3 (DCh)

CMD/Pas	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
RDID3	R	DCh	DC00h	-	ID3[7:0]								-
Description	This read byte identifies the AMOLED module/driver.												
Restriction	-												

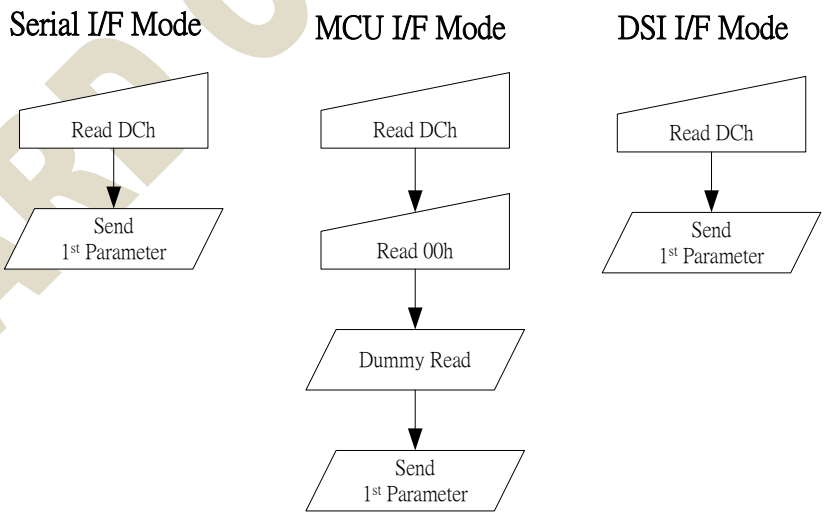
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



9. Electrical Characteristics

9.1. Absolute maximum ratings

Symbol	Parameter	Unit	Value	Note
IOVCC/VCC	Interface Supply Voltage	V	-0.3 to +5.5	Note(3),(4)
VCIR/VCIB	Logic Supply Voltage	V	-0.3 to +5.5	Note(3),(5)
AVDD	Positive Voltage output	V	-0.3 to +6.6	Note(6)
VGH-VGL	Positive Voltage output	V	-0.3 to +33	Note(8)
Top	Operating Temperature	°C	-20 to +85	Note(10)
Tstg	Storage Temperature	°C	-55 to +110	Note(11)

Table 9.1 Absolute maximum ratings

Note: (1) Permanent device damage may occur if absolute maximum conditions are exceeded.
(2) Functional operation should be restricted to the conditions described under DC Characteristics.
(3) IOVCC, VSSD must be maintained.
(4) To make sure IOVCC/VCC ≥ VSSD.
(5) To make sure VCIR/VCIB ≥ AVSS.
(6) To make sure AVDD ≥ AVSS
(7). To make sure VGH ≥ AVSS
(8) To make sure AVSS ≥ VGL (VGH +|VGL| < 33V)
(9) For die and wafer products, specified up to +85℃
(10) This temperature specifications apply to the TCP package.

9.2. DC characteristics

(T_A=-20 ~ 85 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IOVCC	V_{IN}	Interface Supply Voltage	1.65	-	3.6	V
VCI	V_{IN}	Analog Supply Voltage	2.7	-	3.6	V
Input high voltage	V_{IH}	IOVCC= 1.65 ~ 3.3V VCI= 2.6 ~ 3.3V	0.7 $_{IOVCC}$	-	IOVCC	V
Input low voltage	V_{IL}		0	-	0.3 $_{IOVCC}$	V
VOTP	V_{IH} V_{IL}	VOTP	8.0V	8.25V	8.5V	V
Output high voltage (SDO, TE, Swire,TE1)	V_{OH1}	I_{OH} = -1.0 mA	0.8 $_{IOVCC}$	-	IOVCC	V
Output low voltage (SDO, TE , Swire, TE1)	V_{OL1}	IOVCC= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 $_{IOVCC}$	V
Logic High level input current	I_{IH}	RESX, DCX_SCL, CSX, RDX, WRX_SCL	-	-	1	µA
		DB[7…0], SDI, DCX	-	-	1	µA
	I_{IHD}	DB[7…0]	-	-	1	µA
		RESX, DCX, CSX, RDX, WRX_SCL	-1	-		µA
Logic Low level input current	I_{IL}	DB[7…0], SDI, DCX	-1	-		µA
		DB[7…0]	-1	-		µA
	I_{ILD}	VCI=2.8V, IOVCC=1.8V T_A =25°C	-	TBD	-	µA
			-	TBD	-	µA
Current consumption Sleep In mode	I_{IOVCC}					
	I_{VCI}					

Table 9.2 DC characteristic

9.3. AC Characteristics

9.3.1. Reset Input Timing

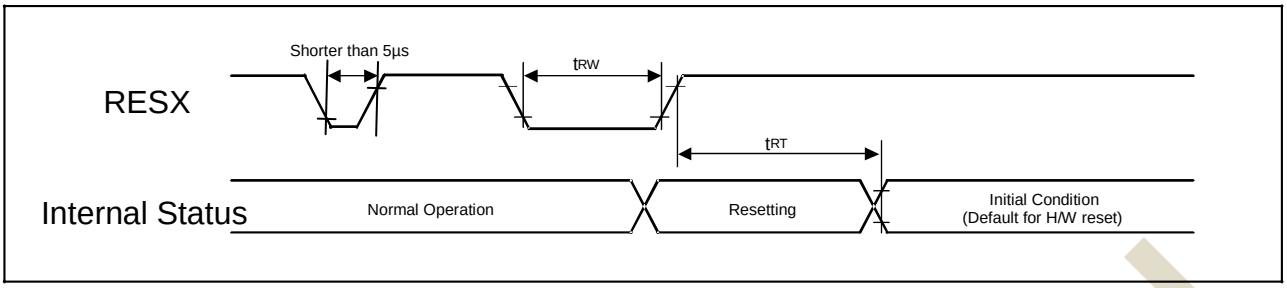


Figure 9.1 Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

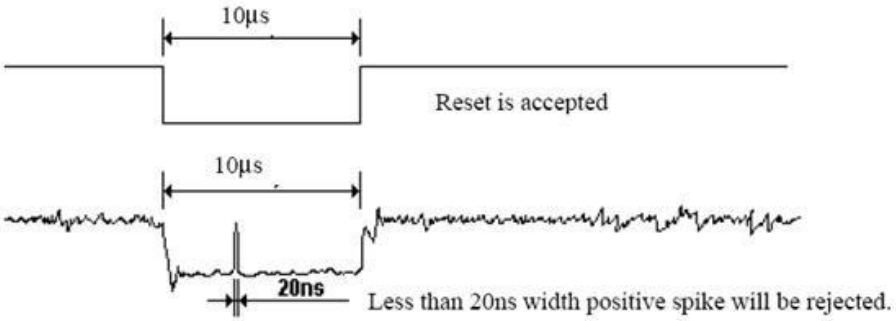
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out command, it is necessary to wait 120msec then send RESX.

Table 9.3 Reset timings

9.3.2. 8080 Series Parallel 8-bit Interface Characteristics

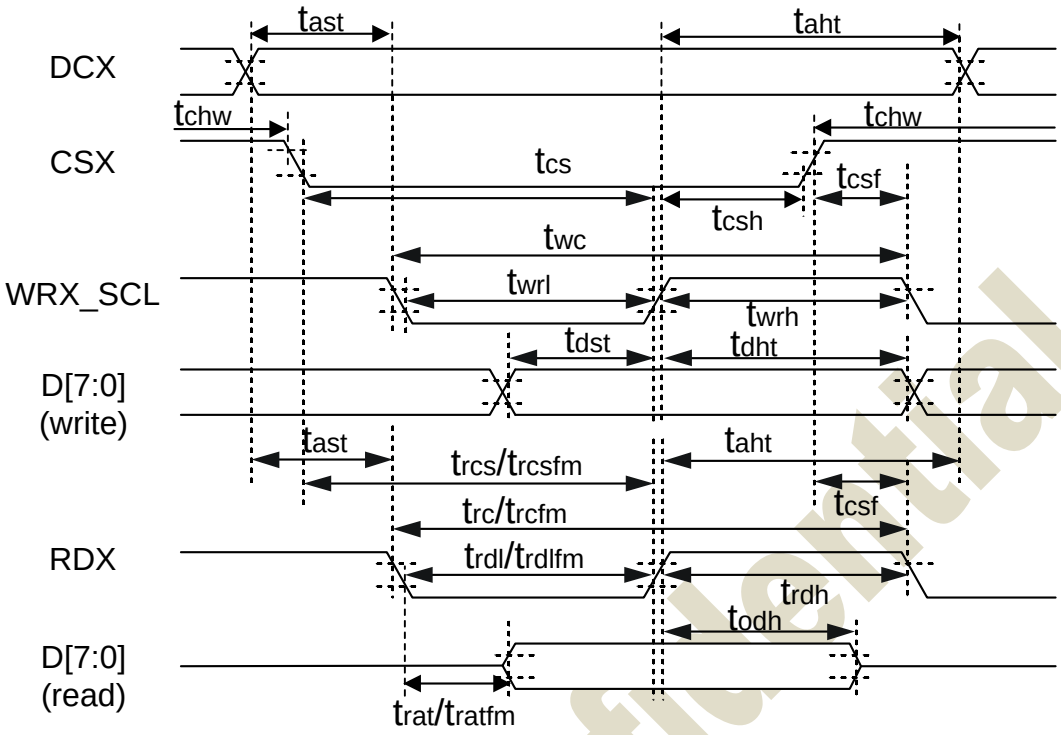


Figure 9.2 8080 Series Parallel interface Timing Characteristics

(T_A=25°C, IOVCC=1.8V, VCI=2.8V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (write/read)	10	-	ns	
CSX	tchw	CSX “H” Pulse Width	0		ns	
	tcs	Chip select setup time (write)	15		ns	
	trcs	Chip select setup time (read ID)	45		ns	
	trcsfm	Chip Select setup time (read FM)	355		ns	
	tcsf	Chip select wait time (write/read)	10		ns	
	tcsh	Chip select hold time	10		ns	
WRX	twc	Write cycle	66		ns	
	twrh	Control pulse “H” duration	15		ns	
	twrl	Control pulse “L” duration	15		ns	
RDX(ID)	trc	Read cycle (ID)	160		ns	
	trdh	Control pulse “H” duration (ID)	90		ns	
	trdl	Control pulse “L” duration (ID)	45		ns	
RDX(FM)	trcfm	Read cycle (FM)	450		ns	
	trdhfm	Control pulse “H” duration (FM)	90		ns	
	trdlfm	Control pulse “L” duration (FM)	355		ns	
D[7:0]	Tdst	Data setup time	10		ns	
	tdht	Data hold time	10		ns	
	trat	Read access time (ID)		42	ns	
	tratfm	Read access time (FM)		340	ns	
	todh	Output disable time	20	80	ns	

Table 9.4 8080 Series Parallel interface AC characteristics

9.3.3. 3-line Serial Interface Timing Characteristics

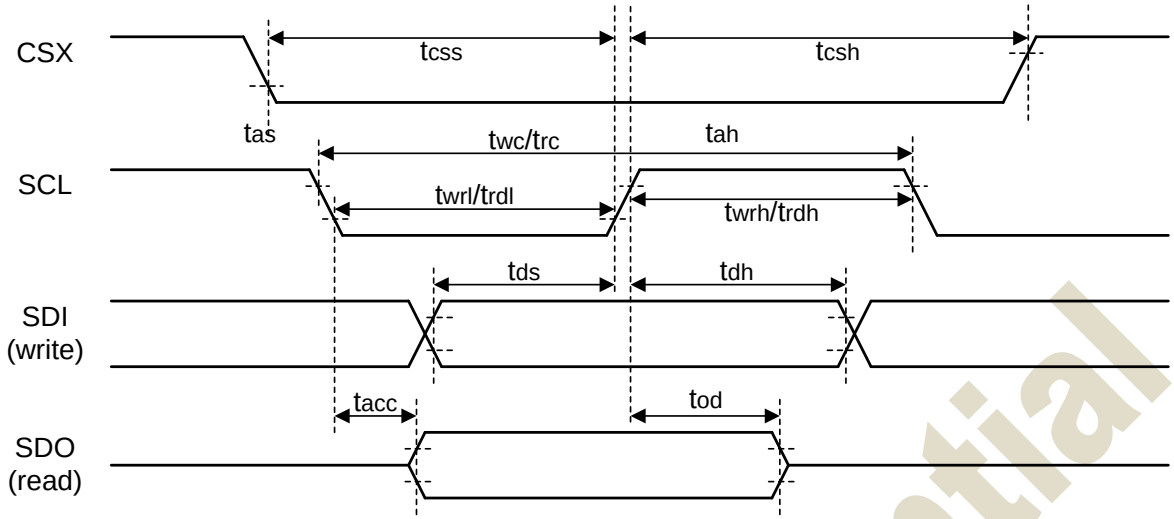


Figure 9.3 3-line Serial Interface Timing Characteristics

(T_A=25°C, IOVCC=1.8V, VCI=2.8V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tcss	Chip select setup time (Write)	15		ns	
	tcsh	Chip select setup time (Read)	60		ns	
SCL (write)	twc	Write cycle	16		ns	
	twrh	Control pulse “H” duration	7		ns	
	twrl	Control pulse “L” duration	7		ns	
SCL (read)	trc	Read cycle	150		ns	
	trdh	Control pulse “H” duration	60		ns	
	trdl	Control pulse “L” duration	60		ns	
SDI/SDO (write)	tds	Data setup time	7		ns	
	tdt	Data hold time	7		ns	
SDI/SDO (read)	tracc	Read access time	10	50	ns	
	tod	Output disable time	15	50	ns	

Table 9.5: 3-line Serial interface AC characteristics

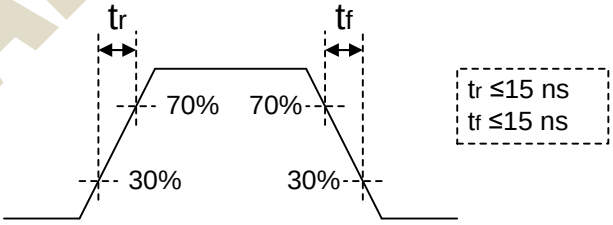


Figure 9.4 Input rise and fall times

9.3.4. Serial Interface Timing Characteristics (4-line SPI)

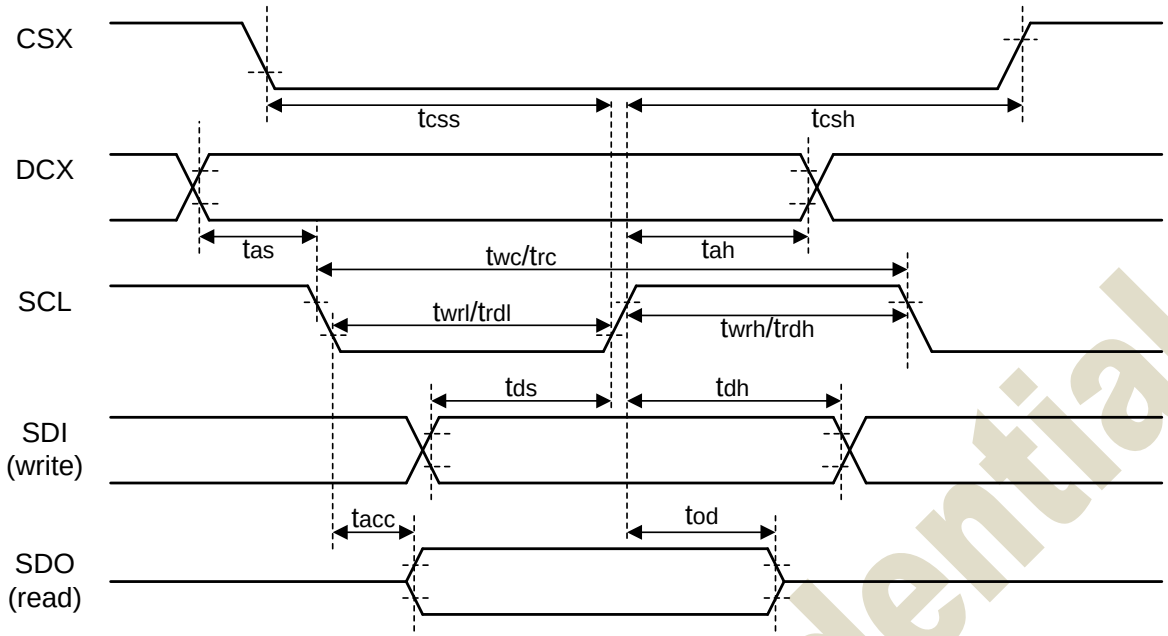


Figure 9.5 4-line Serial Interface Timing Characteristics

(T_A=25°C, IOVCC=1.8V, VCI=2.8V)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tcss	Chip select setup time (Write)	15		ns	
	tcsh	Chip select setup time (Read)	60		ns	
DCX	tas	Address setup time	10		ns	
	tah	Address hold time (Write/Read)	10		ns	
WRX (write)	twc	Write cycle	16		ns	
	twrh	Control pulse “H” duration	7		ns	
	twrl	Control pulse “L” duration	7		ns	
WRX (read)	trc	Read cycle	150		ns	
	trdh	Control pulse “H” duration	60		ns	
	trdl	Control pulse “L” duration	60		ns	
SDI/SDO (write)	tds	Data setup time	7		ns	
	tdt	Data hold time	7		ns	
SDI/SDO (read)	tracc	Read access time	-	50	ns	
	tod	Output disable time	15	50	ns	

Table 9.6 4-line Serial interface AC characteristics

9.3.5. DSI D-PHY electronic characteristics

The Description of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: Low-Power Receiver (LP-RX), High-Speed Receiver (HS-RX), the Low-Power Contention Detector (LP-CD), and Low Power Transmitter (LP-TX). Figure 9.6 shows the complete set of electronic functions required for a fully featured PHY transceiver.

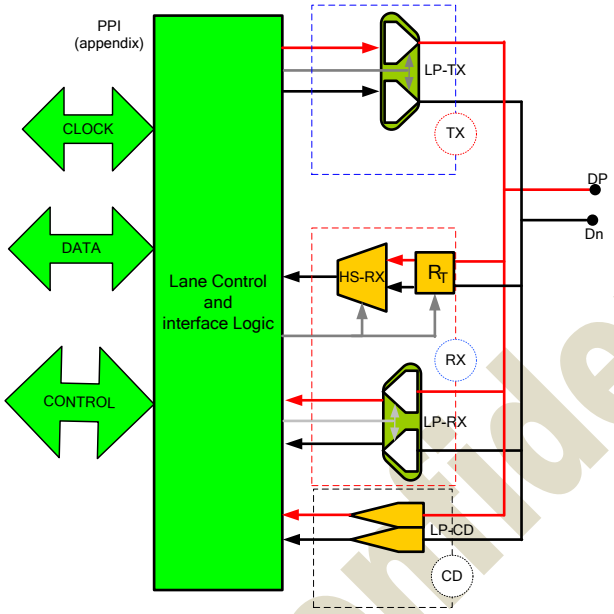


Figure. 9.1 Electronic functions of a D-PHY transceiver

Figure 9.7 shows both the HS and LP signal levels of electronic characteristics, respectively. Where, the HS receiver utilizes low-voltage swing differential signaling. The LP transmitter and LP receiver utilize low-voltage swing single signaling. Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

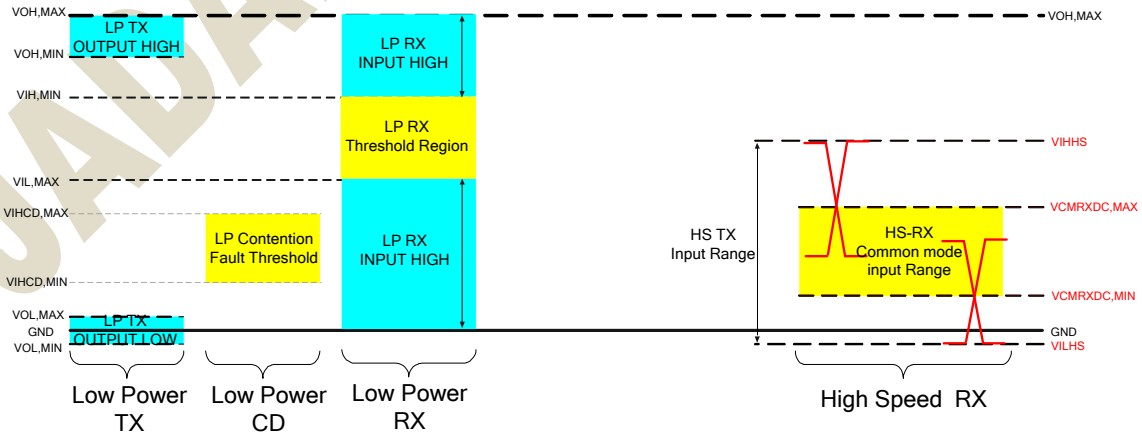


Figure 9.6 HS and LP signal levels

The Electronic Characteristics of Low-Power Transmitter (TX)

The Low-Power TX shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power modes. Hence, it is important to keep static power consumption of a LP TX be as low as possible. Under tables list DC and AC characteristic for Low power transmitter.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 9.7 LP-TX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(2) When the output voltage is between 400 mV and 930 mV.

(3) Measured as average across any 50 mV segment of the output signal transition.

(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.

(5) This value represents a corner point in a piecewise linear curve.

(6) When the output voltage is in the range specified by VPIN(absmax).

(7) When the output voltage is between 400 mV and 700 mV.

(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.

(9) When the output voltage is between 700 mV and 930 mV.

Table 9.8 LP-TX AC Specifications

The Electronic Characteristics of Receiver (RX)

This part includes two parts which Low-Power RX and High-Speed RX. Because they have differential DC and AC characteristic, first to describe LP-RX then describe HS-RX.

Low-Power Receiver (RX)

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The Figure 9.8 shows Input Glitch Rejection of Low-Power RX. In addition, under tables list DC and AC characteristic for LP-RX

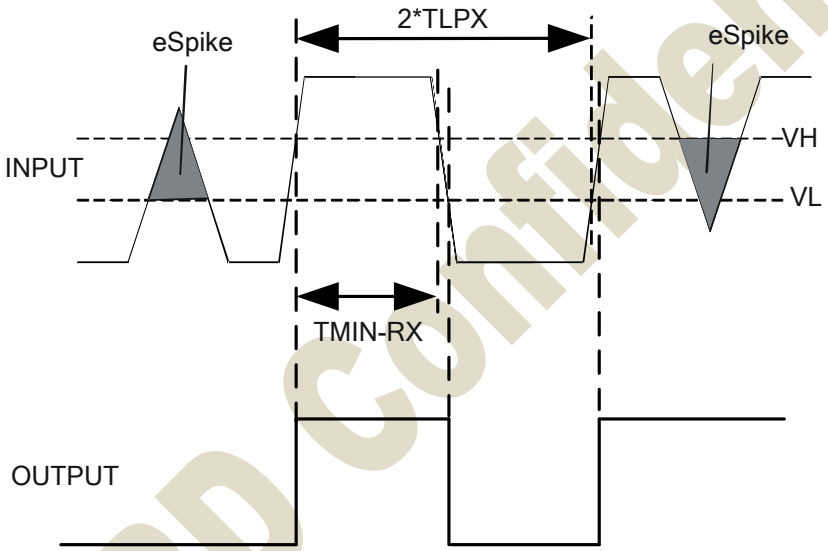


Figure 9.7 Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

Table 9.9 LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 9.10 LP-RX AC Specifications

Line Contention Detection

Contention can be inferred by following conditions:

1. Detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than VIL.
2. Detect an LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than VIHCD.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
$V_{IAMOLED}$	Logic 0 contention threshold	-	-	200	mV	-

Table 9.11 Contention Detector DC Specifications

High-Speed Receiver (RX)

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 9.12 HS Receiver DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 250 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 9.13 HS Receiver AC Specifications

High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 9.9.

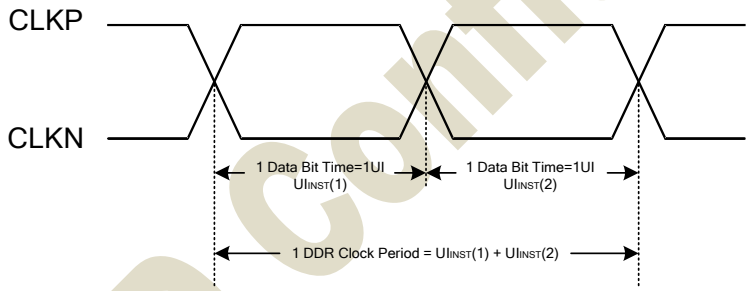


Figure 9.8 DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

(2)The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 220Mbps/per lane @ 1 data lane 24-bit data format.

Table 9.14 Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 9.10 Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

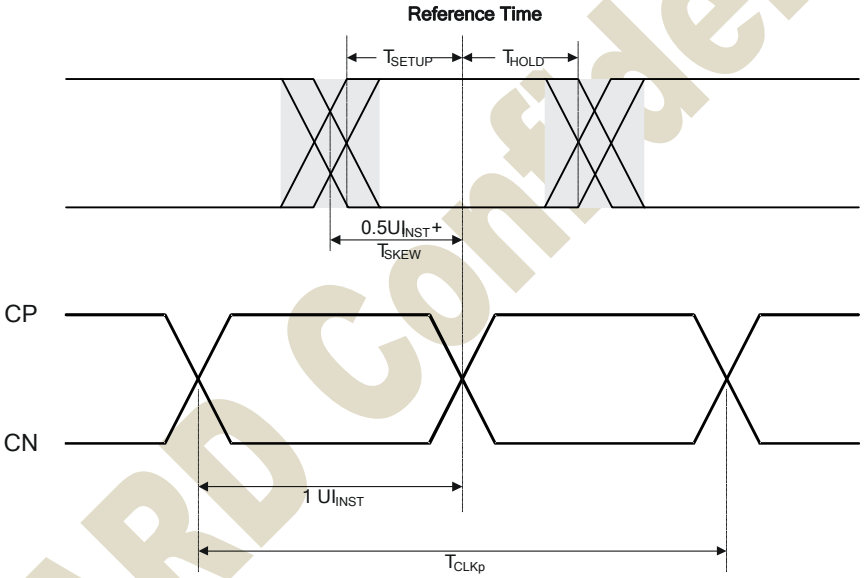


Figure 9.9 Data to Clock Timing Definitions

Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 11.16. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 11.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST

Table 9.15 Data to Clock Timing Specifications

10. Chip Information

10.1. PAD assignment

Chip Size: 8300um * 1290um(Include Scribe-Line and Seal-Ring)